Invalid TXCLK_IN and Initialization Divide Register Combination for UT200SpW4RTR SpaceWire Router

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC*
4-PORT SPACEWIRE ROUTER	UT200SpW4RTR	NA Note 1	NA	WD41A

Note 1: WD41A will not be sold against the SMD. All SMD shipments will be with Rev B Silicon.
*PIC = Product Identification Code

1.0 Overview

Revision A of the 4-Port SpaceWire router contains an anomaly where certain transmit clock in rates (TXCLK_IN) and initialization divide register (TX_DIV[4:0]) values do not properly start the Initialization Sequence as defined in ECSS-E-ST-50-12C, section 8.7.

When the UT200SpW4RTR is powered up, or reset, the link initialization sequence must take place at rate of 10Mbps ±1Mbps. As described in the SpaceWire Standard ECSS-E-ST-50-12C, link initialization is the process by which the two ends of a point-to-point link establish communications. Link initialization is part of the protocol and done automatically within the router by the interaction of the state machine on each side of a SpW link.

After power up or reset the user must know at least one of the TXCLK_IN rates. This clock rate is used to determine TX_DIV[4:0] pins which are loaded into the 0x010F, 0x0110, 0x0111, and 0x0112 initialization divide registers. Once TX_DIV[4:0] is set to the proper value to ensure an initialization rate of 10Mbps ±1Mbps, the link initialization will complete as called out in ECSS-E-ST-50-12C. Table 2 shows the valid TXCLK_IN, and TX_DIV[4:0] combinations that ensure proper initialization.

If an invalid TXCLK_IN and TX_DIV[4:0] combination is selected the UT200SpW4RTR will not initialize properly or be unable to initialize. Table 2 highlights, in grey, the rates and values that will not produce the proper 10Mbps ±1Mbps data rate for the initialization sequence.

TXCLK_IN (Mbps)	TX_DIV[4:0] (HEX)	Initialization Data Rate 10±1Mbps
200	0x14	10
199	0x13	10.47368421
198	0x13	10.42105263
197	0x13	10.36842105
196	0x13	10.31578947
195	0x13	10.26315789
194	0x13	10.21052632
193	0x13	10.15789474
192	0x13	10.10526316
191	0x13	10.05263158
190	0x13	10
189	0x12	10.5
188	0x12	10.44444444
187	0x12	10.38888889
186	0x12	10.33333333
185	0x12	10.27777778
184	0x12	10.22222222
183	0x12	10.16666667
182	0x12	10.11111111
181	0x12	10.05555556
180	0x12	10
179	0x11	10.52941176
178	0x11	10.47058824
177	0x11	10.41176471
176	0x11	10.35294118
175	0x11	10.29411765
174	0x11	10.23529412
173	0x11	10.17647059
172	0x11	10.11764706
171	0x11	10.05882353
170	0x11	10
169	0x10	10.5625
168	0x10	10.5
167	0x10	10.4375
166	0x10	10.375
165	0x10	10.3125
164	0x10	10.25
163	0x10	10.1875
162	0x10	10.125
161	0x10	10.0625
160	0x10	10
159	0x0F	10.6
158	0x0F	10.53333333
157	0x0F	10.46666667
156	0x0F	10.4

155	0x0F	10.33333333
154	0x0F	10.26666667
153	0x0F	10.2
152	0x0F	10.13333333
151	0x0F	10.06666667
150	0x0F	10
149	0x0E	10.64285714
148	0x0E	10.57142857
147	0x0E	10.5
146	0x0E	10.42857143
145	0x0E	10.35714286
144	0x0E	10.28571429
143	0x0E	10.21428571
142	0x0E	10.14285714
141	0x0E	10.07142857
140	0x0E	10
139	0x0D	10.69230769
138	0x0D	10.61538462
137	0x0D	10.53846154
136	0x0D	10.46153846
135	0x0D	10.38461538
134	0x0D	10.30769231
133	0x0D	10.23076923
132	0x0D	10.15384615
131	0x0D	10.07692308
130	0x0D	10
129	0x0C	10.75
128	0x0C	10.66666667
127	0x0C	10.58333333
126	0x0C	10.5
125	0x0C	10.41666667
124	0x0C	10.33333333
123	0x0C	10.25
122	0x0C	10.16666667
121	0x0C	10.08333333
120	0x0C	10
119	0x0B	10.81818182
118	0x0B	10.72727273
117	0x0B	10.63636364
116	0x0B	10.54545455
115	0x0B	10.45454545
114	0x0B	10.36363636
113	0x0B	10.27272727
112	0x0B	10.18181818
111	0x0B	10.09090909
110	0x0B	10
109	0x0A	10.9
108	0x0A	10.8

107	0x0A	10.7
106	0x0A	10.6
105	0x0A	10.5
104	0x0A	10.4
103	0x0A	10.3
102	0x0A	10.2
101	0x0A	10.1
100	0x0A	10
99	0x0A	9.9
98	0x0A	9.8
97	0x09	10.77777778
96	0x09	10.66666667
95	0x09	10.55555556
94	0x09	10.44444444
93	0x09	10.33333333
92	0x09	10.22222222
91	0x09	10.11111111
90	0x09	10
89	0x09	9.888888889
88	0x09	9.777777778
87	0x08	10.875
86	0x08	10.75
85	0x08	10.625
84	0x08	10.5
83	0x08	10.375
82	0x08	10.25
81	0x08	10.125
80	0x08	10
79	0x08	9.875
78	0x08	9.75
77	0x07	11
76	0x07	10.85714286
75	0x07	10.71428571
74	0x07	10.57142857
73	0x07	10.42857143
72	0x07	10.28571429
71	0x07	10.14285714
70	0x07	10
69	0x07	9.857142857
68	0x07	9.714285714
67	0x07	9.571428571
66	0x06	11
65	0x06	10.83333333
64	0x06	10.66666667
63	0x06	10.5
62	0x06	10.33333333
61	0x06	10.16666667
60	0x06	10

59	0x06	9.833333333
58	0x06	9.666666667
57	0x06	9.5
56	0x06	9.333333333
55	0x05	11
54	0x05	10.8
53	0x05	10.6
52	0x05	10.4
51	0x05	10.2
50	0x05	10
49	0x05	9.8
48	0x05	9.6
47	0x05	9.4
46	0x05	9.2
45	0x05	9
44	0x04	11
43	0x04	10.75
42	0x04	10.5
41	0x04	10.25
40	0x04	10
39	0x04	9.75
38	0x04	9.5
37	0x04	9.25
36	0x04	9
35	0x02	17.5
34	0x02	17
33	0x02	16.5
32	0x02	16
31	0x02	15.5
30	0x02	15
29	0x02	14.5
28	0x02	14
27	0x02	13.5
26	0x02	13
25	0x02	12.5
24	0x02	12
23	0x02	11.5
22	0x02	11
21	0x02	10.5
20	0x02	10
19	0x02	9.5
18	0x02	9
17	0x02	8.5
16	0x01	16
15	0x01	15
14	0x01	14
13	0x01	13
12	0x01	12

11	0x01	11
10	0x01	10
9	0x01	9
8	0x01	8
7	0x01	7
6	0x01	6
5	0x01	5
4	0x01	4
3	0x01	3
2	0x01	2
1	0x01	1

Table 2. Valid TXCLK_IN and TX_DIV[4:0] configurations

2.0 Corrective Action

This anomaly can be prevented by ensuring that TXCLK_IN and TX_DIV[4:0] do not fall within any of the values highlighted in grey in Table 2.

3.0 Rev A vs. Rev B

Revision A of the UT200SpW4RTR contains this anomaly. Revision B will correct this errata for the TX_DIV[4:0] = 0x03 options only.