

UT9Q512K32E 16Megabit RadTolerant SRAM MCM

Datasheet

Cobham.com/HiRel

April 2020

The most important thing we build is trust

FEATURES

- ❑ 25ns maximum (5 volt supply) address access time
- ❑ Asynchronous operation for compatible with industry standard 512K x 8 SRAMs
- ❑ TTL compatible inputs and output levels, three-state bidirectional data bus
- ❑ Typical radiation performance:
 - Total dose: 100 krad(Si)
 - SEL Immune: 110 MeV-cm²/mg
 - SEU onset LET_{th}: 2.8 MeV-cm²/mg
 - Saturated Cross Section 2.8E-8 cm²/bit
 - <1.1E-9 errors/bit-day, Adams 90% worst case environment geosynchronous orbit
- ❑ Packaging:
 - 68-lead dual cavity ceramic quad flatpack (CQFP) (11.0 grams)
- ❑ Standard Microcircuit Drawing 5962-01511
 - QML Q & V compliant part

INTRODUCTION

The UT9Q512K32E RadTol product is a high-performance 2M byte (16Mbit) CMOS static RAM multi-chip module (MCM), organized as four individual 524,288 x 8 bit SRAMs with a common output enable. Memory expansion is provided by an active LOW Chip Enable ($\overline{E_n}$), an active LOW Output Enable (\overline{G}), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to each memory is accomplished by taking Chip Enable ($\overline{E_n}$) input LOW and Write Enable ($\overline{W_n}$) inputs LOW. Data on the eight I/O pins (DQ₀ through DQ₇) is then written into the location specified on the address pins (A₀ through A₁₈). Reading from the device is accomplished by taking Chip Enable ($\overline{E_n}$) and Output Enable (\overline{G}) LOW while forcing Write Enable ($\overline{W_n}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The input/output pins are placed in a high impedance state when the device is deselected ($\overline{E_n}$ HIGH), the outputs are disabled (\overline{G} HIGH), or during a write operation ($\overline{E_n}$ LOW and $\overline{W_n}$ LOW). Perform 8, 16, 24 or 32 bit accesses by making $\overline{W_n}$ along with $\overline{E_n}$ a common input to any combination of the discrete memory die.

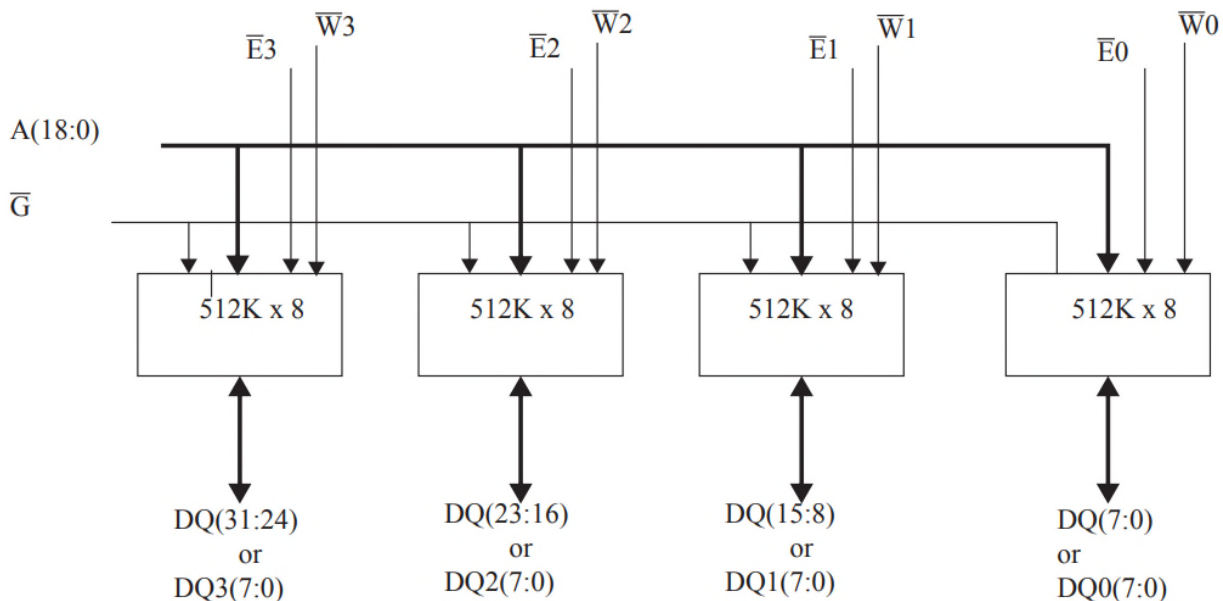


Figure 1. UT9Q512K32E SRAM Block Diagram

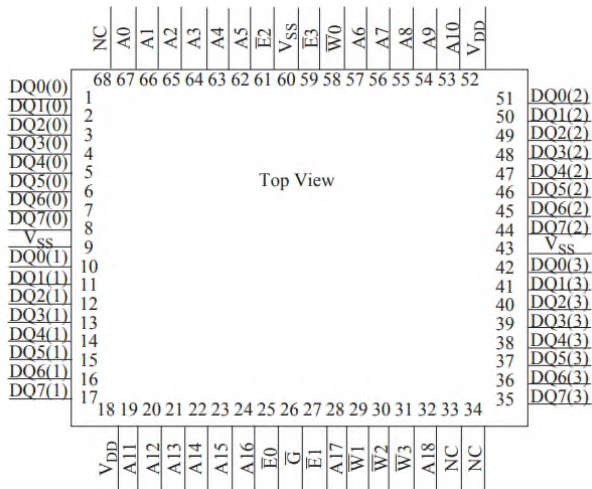


Figure 2. 25ns SRAM Pinout (68)

PIN NAMES

A(18:0)	Address	\overline{Wn}	Write Enable
DQn(7:0)	Data Input/Output	\overline{G}	Output Enable
\overline{En}	Enable	VDD	Power
		VSS	Ground

DEVICE OPERATION

The UT9R512K32E has three control inputs called Chip Enable (\overline{En}), Write Enable (\overline{Wn}), and Output Enable (\overline{G}); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). \overline{En} Device Enable controls device selection, active, and standby modes. Asserting \overline{En} enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. \overline{Wn} controls read and write operations. During a read cycle, \overline{G} must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

\overline{G}	\overline{Wn}	\overline{En}	I/O Mode	Mode
X ¹	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read ²
0	1	0	Data out	Read

Notes:

1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of \overline{Wn} greater than V_{IH} (min) and \overline{En} less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of Device Enable, Output Enable, or valid address to valid data output. Read cycles initiate with the assertion of any chip enable or any address change while any chip enable is asserted.

SRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs while the chip is enabled with \overline{G} asserted and \overline{Wn} deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as Device Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}). Changing addresses prior to satisfying t_{AVAV} minimum results in an invalid operation. Invalid read cycles will require re-initialization.

SRAM Read Cycle 2, the Chip Enable-Controlled Access in Figure 4b, is initiated by \overline{En} going active while \overline{G} remains asserted, \overline{Wn} remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM Read Cycle 3, the Output Enable-Controlled Access in Figure 4c, is initiated by \overline{G} going active while \overline{En} is asserted, \overline{Wn} is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of \overline{Wn} less than $V_{IL}(\max)$ and \overline{En} less than $V_{IL}(\max)$ defines a write cycle. The state of \overline{G} is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either \overline{G} is greater than $V_{IH}(\min)$, or when \overline{Wn} is less than $V_{IL}(\max)$.

Write Cycle 1, the Write Enable-Controlled Access in Figure 5a, is defined by a write terminated by \overline{Wn} going high, with \overline{En} still active. The write pulse width is defined by t_{WLWH} when the write is initiated by \overline{Wn} , and by t_{ETWH} when the write is initiated by \overline{En} . Unless the outputs have been previously placed in the high-impedance state by \overline{G} , the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-Controlled Access in Figure 5b is defined by a write terminated by \overline{En} going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by \overline{Wn} , and by t_{ETEF} when the write is initiated by the \overline{En} going active. For the \overline{Wn} initiated write, unless the outputs have been previously placed in the high-impedance state by \overline{G} , the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

OPERATIONAL ENVIRONMENT

The UT9Q512K32E SRAM incorporates features which allow operation in a limited environment.

Table 2. Operational Environment Design Specifications¹

Total Dose	100	krad(Si)
Heavy Ion Error Rate²	$\leq 1.1E-9$	Errors/Bit-Day
SEL	Immune to 110	MeV-cm ² /mg
SEU Onset LET_{th}	2.8	MeV-cm ² /mg

Notes:

1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

ABSOLUTE MAXIMUM RATINGS¹

(Referenced to VSS)

SYMBOL	PARAMETER	LIMITS
V _{DD}	DC supply voltage	-0.5 to 7.0V
V _{I/O}	Voltage on any pin	-0.5 to 7.0V
T _{STG}	Storage temperature	-65 to +150°C
P _D	Maximum power dissipation	1.0W (per byte)
T _J	Maximum junction temperature ²	+150°C
Θ _{JC}	Thermal resistance, junction-to-case ³	10°C/W
I _I	DC input current	±10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V _{DD}	Positive supply voltage	4.5 to 5.5V
T _C	Case temperature range	(W) Screen -40 to +105°C
V _{IN}	DC input voltage	0V to V _{DD}

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

-40°C to +105°C ($V_{DD} = 5.0V \pm 10\%$ for (W) screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage	(TTL)	2.0		V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL1}	Low-level output voltage	$I_{OL} = 8mA, V_{DD} = 4.5V$ (TTL)		0.4	V
V_{OL2}	Low-level output voltage	$I_{OL} = 200\mu A, V_{DD} = 4.5V$ (CMOS)		0.08	V
V_{OH1}	High-level output voltage	$I_{OH} = -4mA, V_{DD} = 4.5V$ (TTL)	2.4		V
V_{OH2}	High-level output voltage	$I_{OH} = -200\mu A, V_{DD} = 4.5V$ (CMOS)	3.0		V
C_{IN1}^1	Input capacitance; All address and output enable pins	$f = 1MHz @ 0V$		45	pF
C_{IN2}^1	Input capacitance; All enable and write enable pins	$f = 1MHz @ 0V$		18	pF
C_{IO}^1	Bidirectional I/O capacitance	$f = 1MHz @ 0V$		25	pF
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$ and $V_{SS}, V_{DD} = V_{DD} (max)$	-2	2	μA
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ and V_{SS} $V_{DD} = V_{DD} (max)$ $\overline{G} = V_{DD} (max)$	-2	2	μA
$I_{OS}^{2,3}$	Short-circuit output current	$V_{DD} = V_{DD} (max), V_O = V_{DD}$ $V_{DD} = V_{DD} (max), V_O = 0V$	-90	90	mA
$I_{DD}(OP)$	Supply current operating @ 1MHz (per byte)	Inputs: $V_{IL} = 0.8V,$ $V_{IH} = 2.0V$ $I_{OUT} = 0mA$ $V_{DD} = V_{DD} (max)$		40	mA
$I_{DD1}(OP)$	Supply current operating @40MHz (per byte)	Inputs: $V_{IL} = 0.8V,$ $V_{IH} = 2.0V$ $I_{OUT} = 0mA$ $V_{DD} = V_{DD} (max)$		70	mA
$I_{DD2}(SB)$	Supply current standby @0MHz (per byte)	Inputs: $V_{IL} = V_{SS}$ $I_{OUT} = 0mA$ $\overline{E} = V_{DD} - 0.5$ $V_{DD} = V_{DD} (max)$ $V_{IH} = V_{DD} - 0.5V$	-40°C, 25°C	16	mA
			105°C	24	mA

Notes:

* Post-irradiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

-40°C to +105°C ($V_{DD} = 5.0V \pm 10\%$ for (W) screening)

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{AVAV}^{1,6}$	Read cycle time	25		ns
t_{AVSK}^5	Address valid to address valid skew time		4	ns
t_{AVQV}	Read access time		25	ns
t_{AXQX}^2	Output hold time	3		ns
t_{GLQX}^2	\overline{G} -controlled Output Enable time	0		ns
t_{GLQV}	\overline{G} -controlled Output Enable time (Read Cycle 3)		10	ns
t_{GHQZ}^2	\overline{G} -controlled output three-state time		10	ns
$t_{ETQX}^{2,3}$	$\overline{E}n$ -controlled Output Enable time	3		ns
t_{AVET2}^5	Address setup time for read ($\overline{E}n$ -controlled)	-4		ns
t_{ETQV}^3	$\overline{E}n$ -controlled access time		25	ns
$t_{EFQZ}^{1,2,4}$	$\overline{E}n$ -controlled output three-state time		10	ns

Notes:

* Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Functional test.

2. Three-state is defined as a 500mV change from steady-state output voltage.

3. The ET (chip enable true) notation refers to the latter falling edge of $\overline{E}n$. SEU immunity does not affect the read parameters.

4. The EF (chip enable false) notation refers to the latter rising edge of $\overline{E}n$. SEU immunity does not affect the read parameters.

5. Guaranteed by design

6. Address changes prior to satisfying t_{AVAV} minimum is an invalid operation

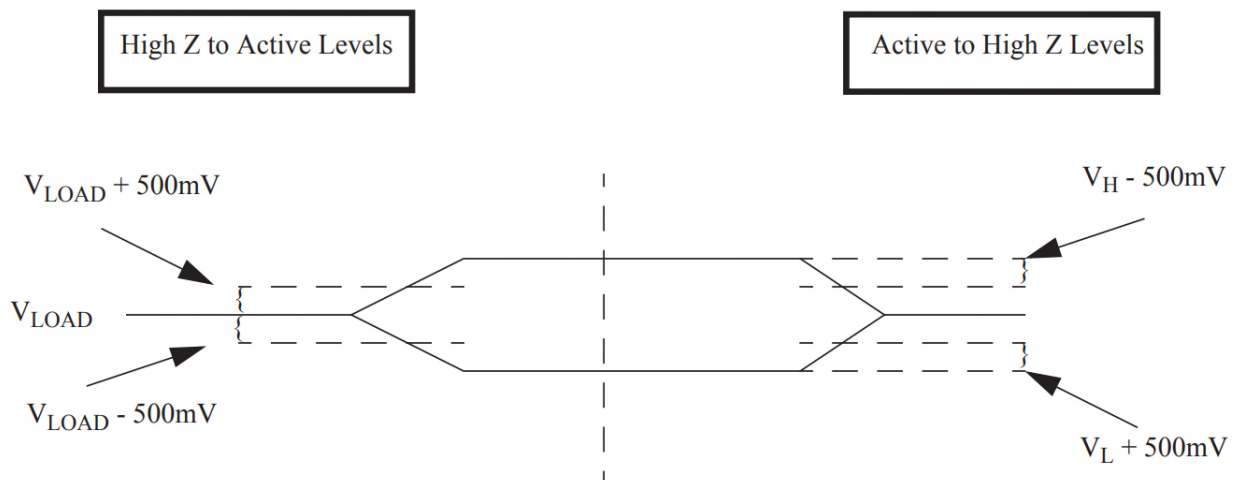


Figure 3. 5-Volt SRAM Loading

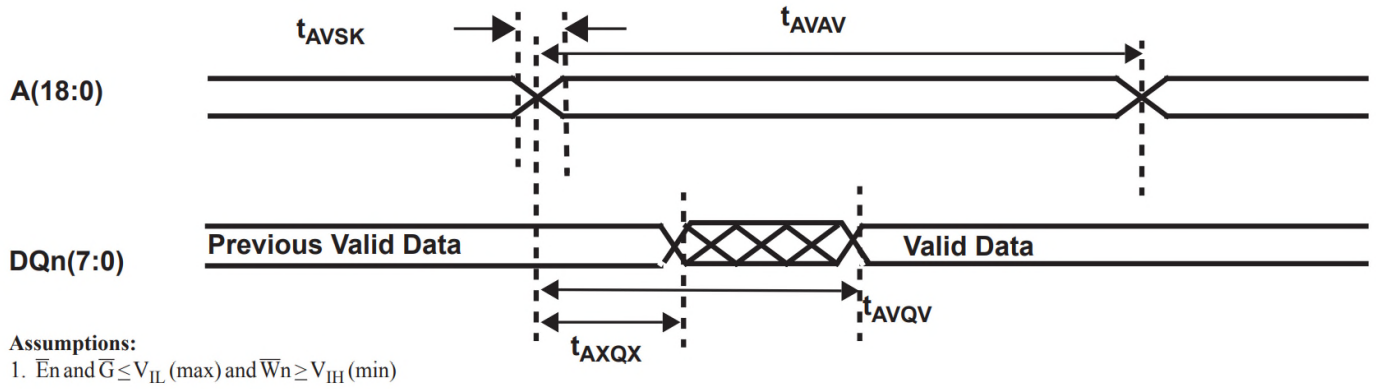
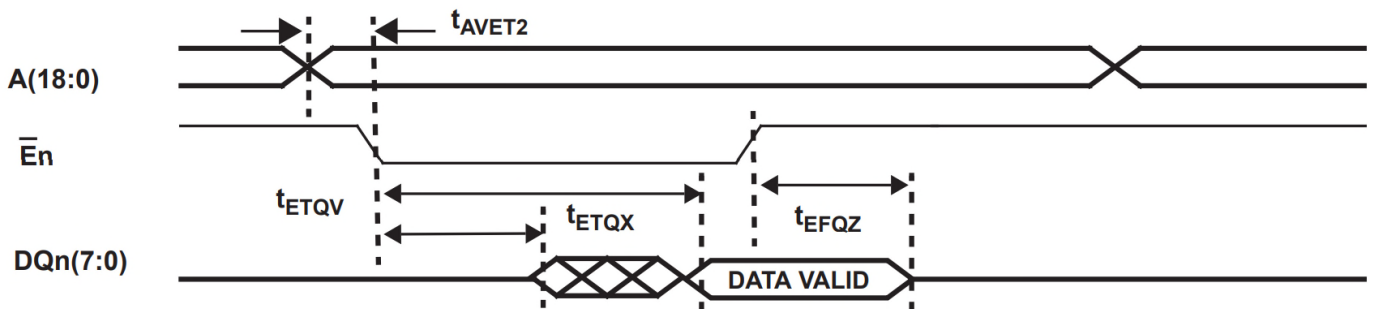
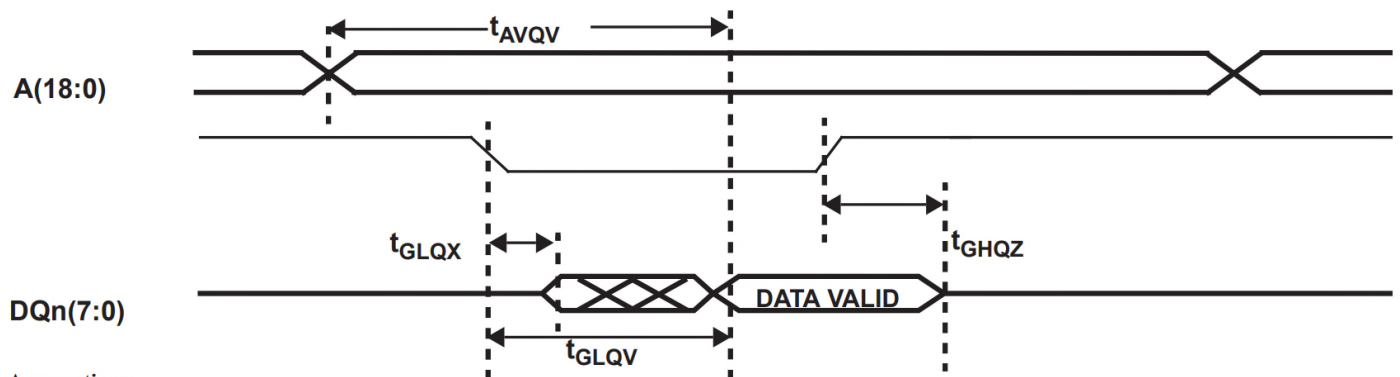


Figure 4a. SRAM Read Cycle 1: Address Access



Assumptions:
 1. $\bar{G} \leq V_{IL}(\text{max})$ and $\bar{W}_n \geq V_{IH}(\text{min})$

Figure 4b. SRAM Read Cycle 2: Chip Enable-Controlled Access



Assumptions:
 1. $\bar{E}_n \leq V_{IL}(\text{max})$ and $\bar{W}_n \geq V_{IH}(\text{min})$

Figure 4c. SRAM Read Cycle 3: Output Enable-Controlled Access

AC CHARACTERISTICS WRITE CYCLE (Pre/Post-Radiation)*

-40°C to +105°C ($V_{DD} = 5.0V \pm 10\%$ for (W) screening)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}^1	Write cycle time	25		ns
t_{ETWH}	Device Enable to end of write	20		ns
t_{AVET}	Address setup time for write ($\overline{E}n$ - controlled)	1		ns
t_{AVWL}	Address setup time for write ($\overline{W}n$ - controlled)	0		ns
t_{WLWH}	Write pulse width	20		ns
t_{WHAX}	Address hold time for write ($\overline{W}n$ - controlled)	0		ns
t_{EFAX}	Address hold time for Device Enable ($\overline{E}n$ - controlled)	0		ns
t_{WLQZ}^2	$\overline{W}n$ - controlled three-state time		10	ns
t_{WHQX}^2	$\overline{W}n$ - controlled Output Enable time	5		ns
t_{ETEF}	Device Enable pulse width ($\overline{E}n$ - controlled)	20		ns
t_{DVWH}	Data setup time	15		ns
t_{WHDX}	Data hold time	2		ns
t_{WLEF}	Device Enable controlled write pulse width	20		ns
t_{DVEF}	Data setup time	15		ns
t_{EFDX}	Data hold time	2		ns
t_{AVWH}	Address valid to end of write	20		ns
t_{WHWL}^1	Write disable time	5		ns

Notes:

*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019

1. Functional test performed with outputs disabled (\overline{G} high).
2. Three-state is defined as 500mV change from steady-state output voltage (see Figure 3).

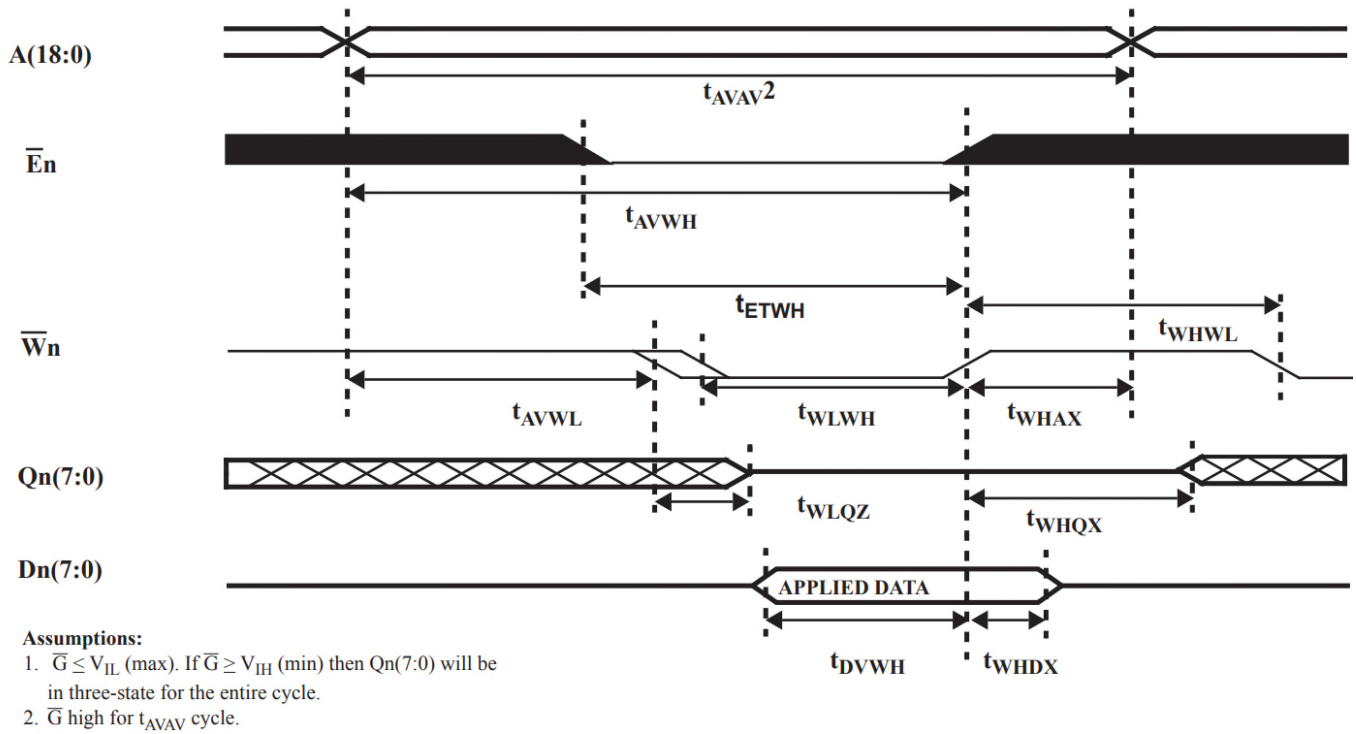


Figure 5a. SRAM Write Cycle 1: Write Enable – Controlled Access

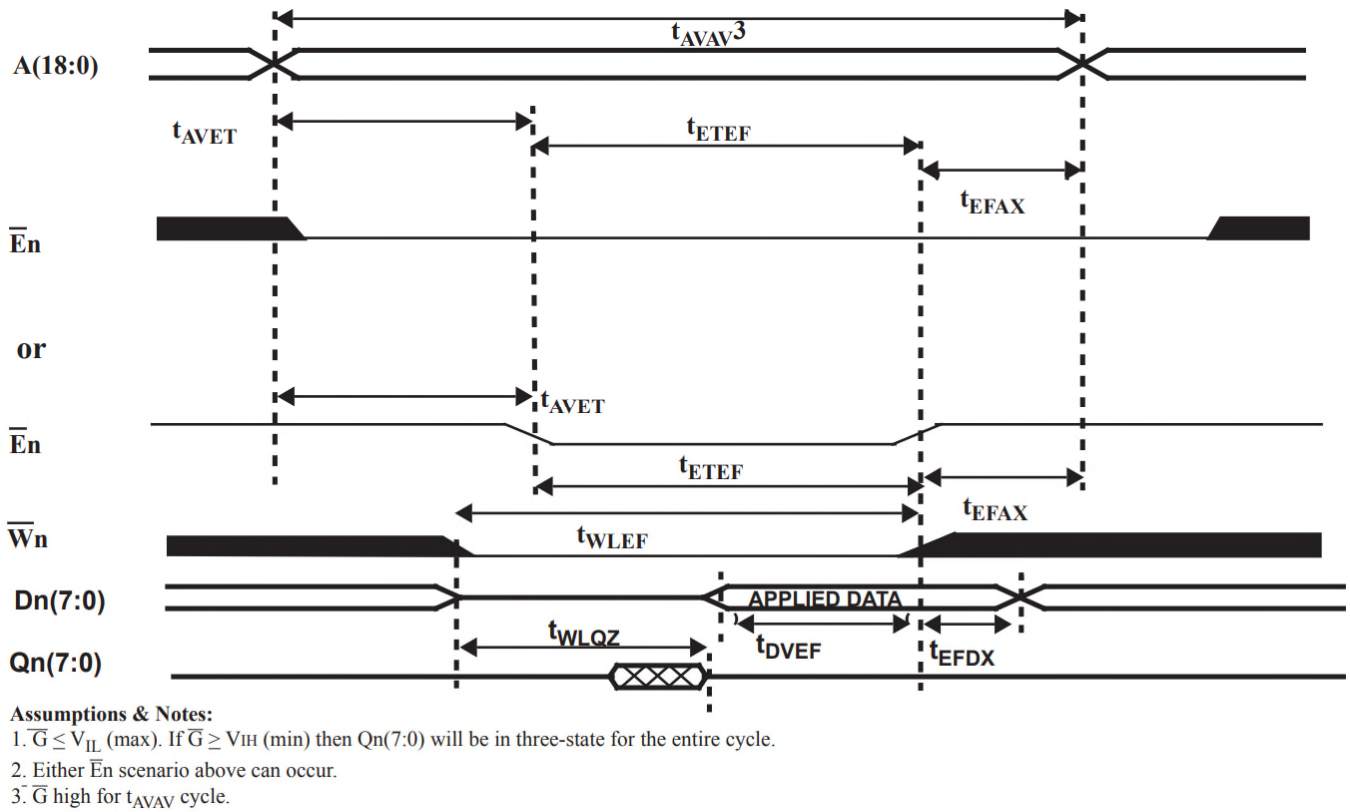


Figure 5b. SRAM Write Cycle 2: Chip Enable - Controlled Access

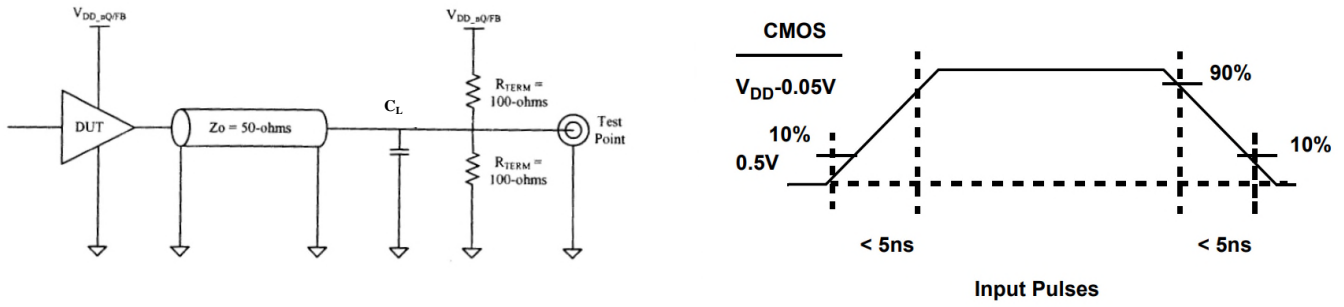


Figure 6. AC Test Loads and Input Waveforms

Notes:

1. 50pF including scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD}/2$).

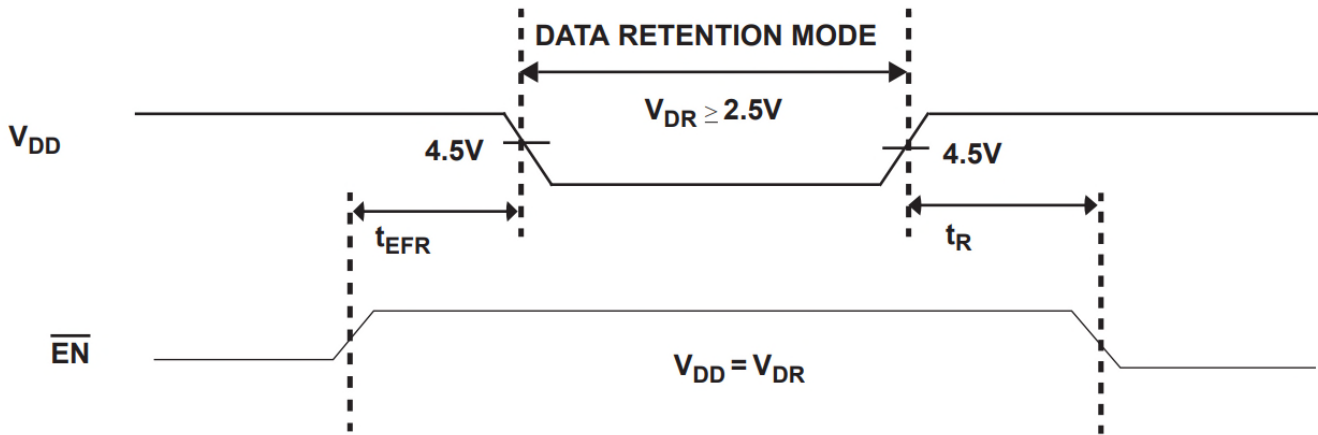


Figure 7. Low V_{DD} Data Retention Waveform

DATA RETENTION CHARACTERISTICS (Pre-Radiation)*

($V_{DD} = V_{DD}(\min)$, 1 Sec DR Pulse)

SYMBOL	PARAMETER	TEMP	MINIMUM	MAXIMUM	UNIT
V_{DR}	VDD for data retention	--	2.5	--	V
I_{DDR}^1	Data retention current (per byte)	-40°C	--	16	mA
		25°C	--	16	mA
		105°C	--	24	mA
$t_{EFR}^{1,2}$	Chip deselect to data retention time	--	0	--	ns
$t_R^{1,2}$	Operation recovery time	--	t_{AVAV}	--	ns

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. $\overline{EN} = V_{DR}$ all other inputs = V_{DR} or V_{SS}

2. Not guaranteed or tested

Packaging

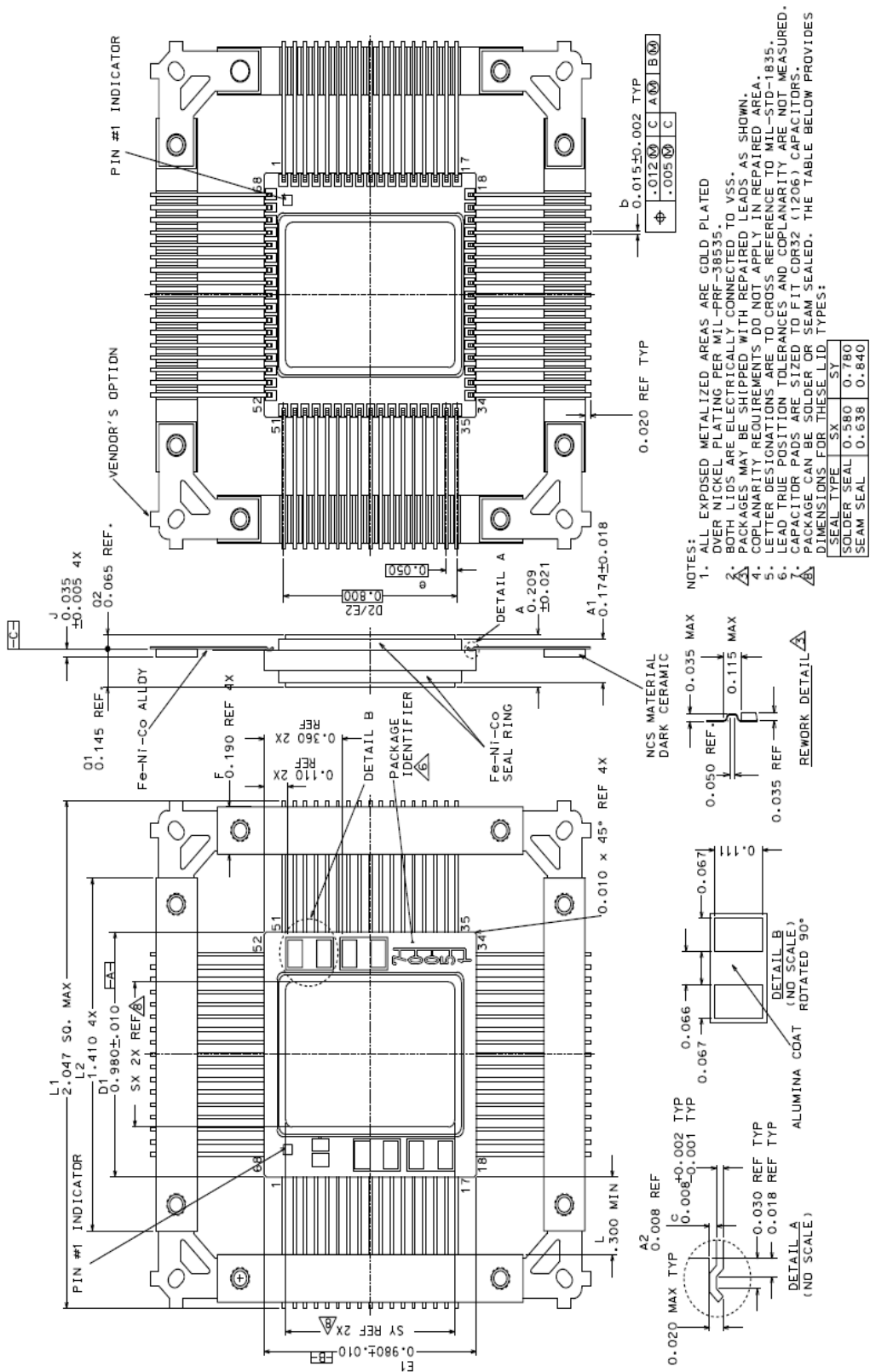
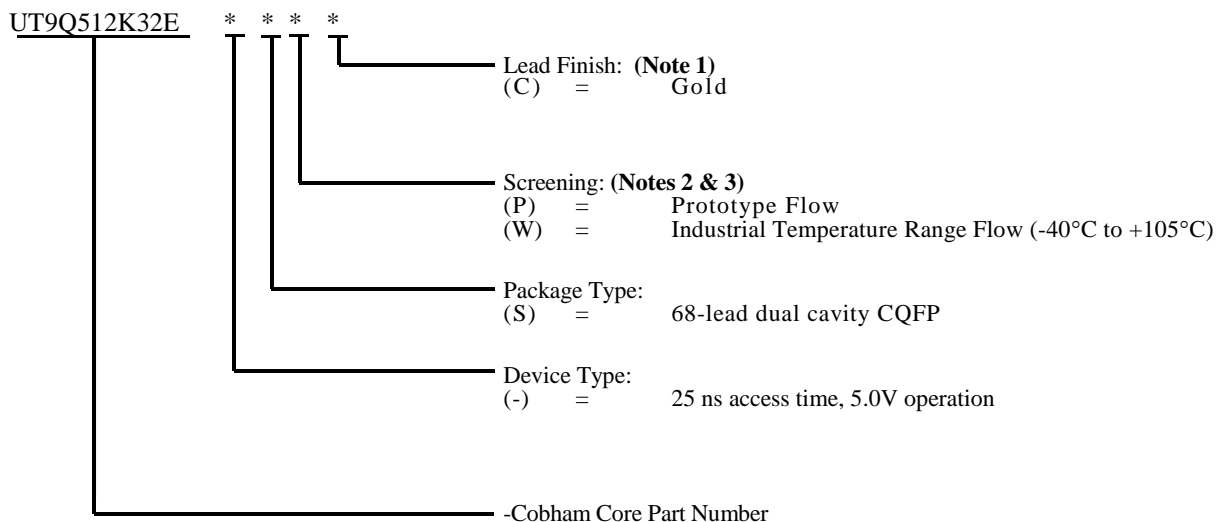


Figure 8. 68-Lead Ceramic Quad Flatpack

ORDERING INFORMATION

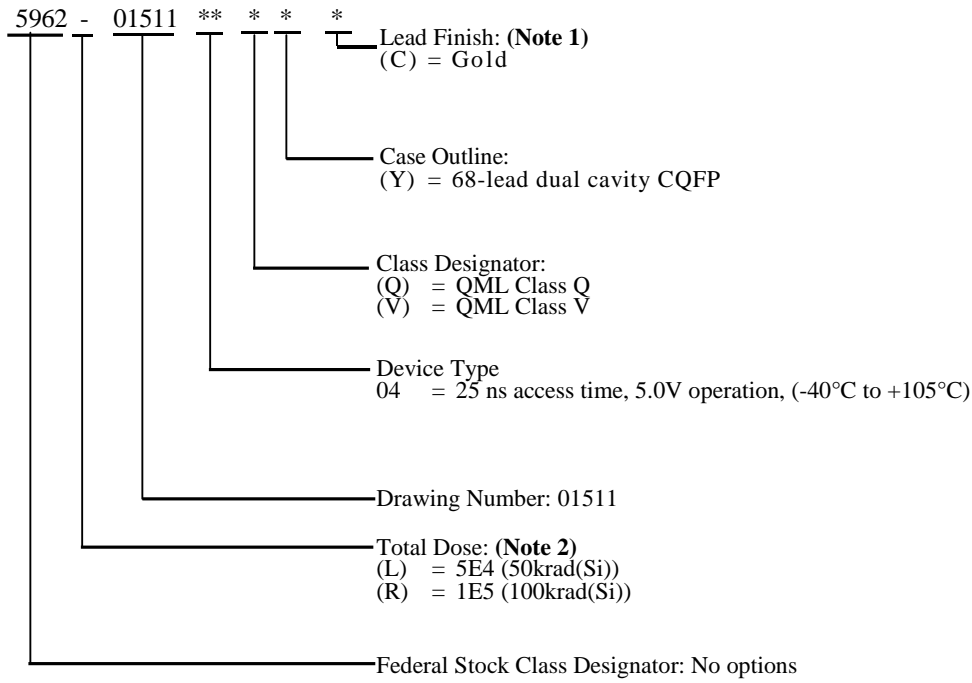
512K32E 16Megabit SRAM MCM:



Notes:

- 1. Gold lead finish only.
- 2. Prototype flow per Cobham Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Radiation neither tested nor guaranteed.
- 3. Extended Industrial Range flow per Cobham Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C to 105°C. Radiation neither tested nor guaranteed.

512K32E 16 Megabit SRAM MCM: SMD



Notes:

1. Lead finish is "C" (Gold) only.
2. Total dose radiation must be specified when ordering.

NOTES

Cobham Semiconductor Solutions – Datasheet Definitions

Advanced Datasheet - Product In Development (datasheet subject to change)

Preliminary Datasheet – Product in Characterization and Shipping Prototypes (datasheet subject to change)

Datasheet – Product in Production

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

**Cobham Advanced Electronic Solutions
Semiconductor & Space Solutions
4350 Centennial Blvd
Colorado Springs, CO 80907**

The logo for Cobham, featuring the word "COBHAM" in a bold, italicized, sans-serif font.

**E: Info-HiRel@cobham.com
T: 800 645 8862**

Cobham Colorado Springs Inc (Cobham) reserves the right to make changes to any products and services described herein at any time without notice. Consult Cobham or an authorized sales representative to verify that the information in this data sheet is current before using this product. Cobham does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing by Cobham; nor does the purchase, lease, or use of a product or service from Cobham convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual rights of Cobham or of third parties

REVISION HISTORY

Date	Revision	Change Description
July 15, 2019	A	Changed template to Cobham from Aeroflex
April 2020	B	Raised max TID to 100krads (Si); Typo fixes; Split input capacitance to clarify capacitance differences between bussed inputs and single inputs; Increased standby current to 16mA; added note to data retention table (pg 11); change package identification marking on package outline; revised SMD PN buildup page to reflect new device type and TID offering; corrected error in test load figure 6