

The most important thing we build is trust

## FEATURES

- ❑ 20ns maximum (3.3 volt supply) address access time
- ❑ Asynchronous operation for compatibility with industry-standard 512K x 8 SRAMs
- ❑ TTL compatible inputs and output levels, three-state bidirectional data bus
- ❑ Operational environment:
  - Total dose: 100 krads(Si)
  - SEL Immune 110 MeV-cm<sup>2</sup>/mg
  - SEU Onset LET<sub>th</sub>: 2.8 MeV-cm<sup>2</sup>/mg
  - Saturated Cross Section 2.8E-8 cm<sup>2</sup>/bit
  - <1.1E-9 errors/bit-day, Adams 90% worst case environment geosynchronous orbit
- ❑ Packaging:
  - 36-lead ceramic flatpack (3.831 grams)
- ❑ Standard Microcircuit Drawing 5962-99607
  - QML Q & V compliant part

## INTRODUCTION

The UT8Q512E RadTol product is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\bar{E}$ ), an active LOW Output Enable ( $\bar{G}$ ), and three-state drivers.

Writing to the device is accomplished by taking Chip Enable ( $\bar{E}$ ) and Write Enable ( $\bar{W}$ ) inputs LOW. Data on the eight I/O pins (DQ0 through DQ7) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by taking Chip Enable ( $\bar{E}$ ) and Output Enable ( $\bar{G}$ ) LOW while forcing Write Enable ( $\bar{W}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (DQ0 through DQ7) are placed in high impedance state when the device is deselected ( $\bar{E}$  HIGH), the outputs are disabled ( $\bar{G}$  HIGH), or during a write operation ( $\bar{E}$  LOW and  $\bar{W}$  LOW)).

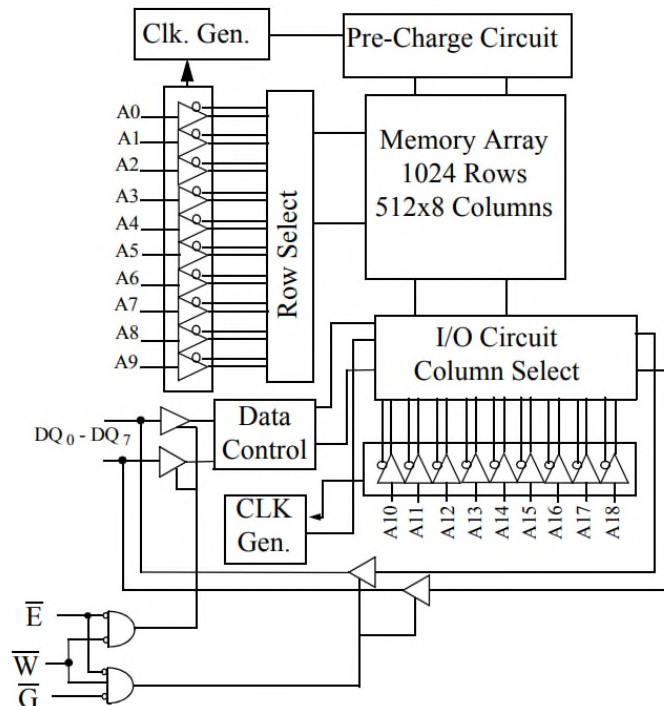


Figure 1. UT8Q512E SRAM Block Diagram

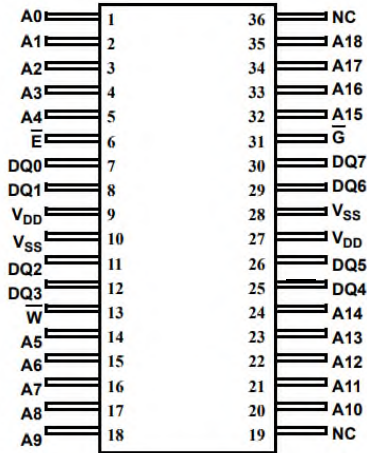


Figure 2. UT8Q512E 20ns SRAM Pinout (36)

### PIN NAMES

A(18:0)	Address
DQ(7:0)	Data Input/Output
$\bar{E}$	Chip Enable
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
V <sub>DD</sub>	Power
V <sub>SS</sub>	Ground

## DEVICE OPERATION

The UT8R512E has three control inputs called Chip Enable ( $\bar{E}$ ), Write Enable ( $\bar{W}$ ), and Output Enable ( $\bar{G}$ ); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0).  $\bar{E}$  controls device selection, active, and standby modes. Asserting  $\bar{E}$  enables the device, causes  $I_{DD}$  to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory.  $\bar{W}$  controls read and write operations. During a read cycle,  $\bar{G}$  must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\bar{G}$	$\bar{W}$	$\bar{E}$	I/O Mode	Mode
X <sup>1</sup>	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read <sup>2</sup>
0	1	0	Data out	Read

#### Notes:

1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

## READ CYCLE

A combination of  $\bar{W}$  greater than  $V_{IH}$  (min) and  $\bar{E}$  less than  $V_{IL}$  (max) defines a read cycle. Read access time is measured from the latter of Chip Enable, Output Enable, or valid address to valid data output. Read cycles initiate with the assertion of chip enable or any address input change while chip enable is asserted.

SRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs while the chip is enabled with  $\bar{G}$  asserted and  $\bar{W}$  deasserted. Valid data appears on data outputs DQ(7:0) after the specified  $t_{AVQV}$  is satisfied. Outputs remain active throughout the entire cycle. As long as Chip Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time ( $t_{AVAV}$ ). Changing addresses prior to satisfying  $t_{AVAV}$  minimum results in an invalid operation. Invalid read cycles will require re-initialization.

SRAM Read Cycle 2, the Chip Enable-Controlled Access in Figure 4b, is initiated by  $\bar{E}$  going active while  $\bar{G}$  remains asserted,  $\bar{W}$  remains deasserted, and the addresses remain stable for the entire cycle. After the specified  $t_{ETQV}$  is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM Read Cycle 3, the Output Enable-Controlled Access in Figure 4c, is initiated by  $\bar{G}$  going active while  $\bar{E}$  is asserted,  $\bar{W}$  is deasserted, and the addresses are stable. Read access time is  $t_{GLQV}$  unless  $t_{AVQV}$  or  $t_{ETQV}$  have not been satisfied.

## WRITE CYCLE

A combination of  $\bar{W}$  less than  $V_{IL}(\max)$  and  $\bar{E}$  less than  $V_{IL}(\max)$  defines a write cycle. The state of  $\bar{G}$  is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either  $\bar{G}$  is greater than  $V_{IH}(\min)$ , or when  $\bar{W}$  is less than  $V_{IL}(\max)$ .

Write Cycle 1, the Write Enable-Controlled Access in Figure 5a, is defined by a write terminated by  $\bar{W}$  going high, with  $\bar{E}$  still active. The write pulse width is defined by  $t_{WLWH}$  when the write is initiated by  $\bar{W}$ , and by  $t_{ETWH}$  when the write is initiated by  $\bar{E}$ . Unless the outputs have been previously placed in the high-impedance state by  $\bar{G}$ , the user must wait  $t_{WLQZ}$  before applying data to the nine bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-Controlled Access in Figure 5b is defined by a write terminated by  $\bar{E}$  going inactive. The write pulse width is defined by  $t_{WLEF}$  when the write is initiated by  $\bar{W}$ , and by  $t_{ETEF}$  when the write is initiated by the  $\bar{E}$  going active. For the  $\bar{W}$  initiated write, unless the outputs have been previously placed in the high-impedance state by  $\bar{G}$ , the user must wait  $t_{WLQZ}$  before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

## OPERATIONAL ENVIRONMENT

**Table 2. Operational Environment Design Specifications<sup>1</sup>**

Total Dose	100	krad(Si)
Heavy Ion Error Rate <sup>2</sup>	$\leq 1.1E-9$	Errors/Bit-Day
SEL	Immune to 110	MeV-cm <sup>2</sup> /mg
SEU Onset LETth	2.8	MeV-cm <sup>2</sup> /mg

### Notes:

1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. Adam’s 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

(Referenced to VSS)

SYMBOL	PARAMETER	LIMITS
V <sub>DD</sub>	DC supply voltage	-0.5 to 4.6V
V <sub>I/O</sub>	Voltage on any pin	-0.5 to 4.6V
T <sub>STG</sub>	Storage temperature	-65 to +150°C
P <sub>D</sub>	Maximum power dissipation	1.0W
T <sub>J</sub>	Maximum junction temperature <sup>2</sup>	+150°C
Θ <sub>JC</sub>	Thermal resistance, junction-to-case	10°C/W
I <sub>I</sub>	DC input current	±10 mA

**Notes:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS
V <sub>DD</sub>	Positive supply voltage	3.0 to 3.6V
T <sub>C</sub>	Case temperature range	(C) Screening: -55 to +125°C
V <sub>IN</sub>	DC input voltage	0V to V <sub>DD</sub>

**DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)\***

-55°C to +125°C for (C) screening ( $V_{DD} = 3.3V \pm 0.3V$ )

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
$V_{IH}$	High-level input voltage	(TTL)	2		V
$V_{IL}$	Low-level input voltage	(TTL)		0.8	V
$V_{OL1}$	Low-level output voltage	$I_{OL} = 6mA, V_{DD} = 3.0V$ (TTL)		0.4	V
$V_{OL2}$	Low-level output voltage	$I_{OL} = 200\mu A, V_{DD} = 3.0V$ (CMOS)		0.08	V
$V_{OH1}$	High-level output voltage	$I_{OH} = -3mA, V_{DD} = 3.0V$ (TTL)	2.2		V
$V_{OH2}$	High-level output voltage	$I_{OH} = -200\mu A, V_{DD} = 3.0V$ (CMOS)	$0.8 * V_{DD}$		V
$C_{IN1}$	Input capacitance	$f = 1MHz @ 0V$		14	pF
$C_{IO1}$	Bidirectional I/O capacitance	$f = 1MHz @ 0V$		16	pF
$I_{IN}$	Input leakage current	$V_{IN} = V_{DD}$ and $V_{SS}, V_{DD} = V_{DD} (max)$	-2	2	$\mu A$
$I_{OZ}$	Three-state output leakage current	$V_O = V_{DD}$ and $V_{SS}$ $V_{DD} = V_{DD} (max)$ $\bar{G} = V_{DD} (max)$	-2	2	$\mu A$
$I_{OS}^{2,3}$	Short-circuit output current	$V_{DD} = V_{DD} (max), V_O = V_{DD}$ $V_{DD} = V_{DD} (max), V_O = 0V$	-90	90	mA
$I_{DD(OP)}^4$	Supply current operating @ 1MHz	Inputs: $V_{IL} = 0.8V,$ $V_{IH} = 2.0V$ $I_{OUT} = 0mA$ $V_{DD} = V_{DD} (max)$		50	mA
$I_{DD(OP)}^4$	Supply current operating @ 50MHz	Inputs: $V_{IL} = 0.8V,$ $V_{IH} = 2.0V$ $I_{OUT} = 0mA$ $V_{DD} = V_{DD} (max)$		76	mA
$I_{DD(SB)}^5$	Supply current standby @ 0MHz	Inputs: $V_{IL} = V_{SS}$ $I_{OUT} = 0mA$ $\bar{E} = V_{DD} - 0.5$ $V_{DD} = V_{DD} (max)$ $V_{IH} = V_{DD} - 0.5V$	-55°C, 25°C	16	mA
			125°C	45	mA

**Notes:**

\* Post-irradiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4.  $\bar{G} = V_{IH}$
5. Post-radiation limits are the 125°C temperature limits when specified.

**AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)\***

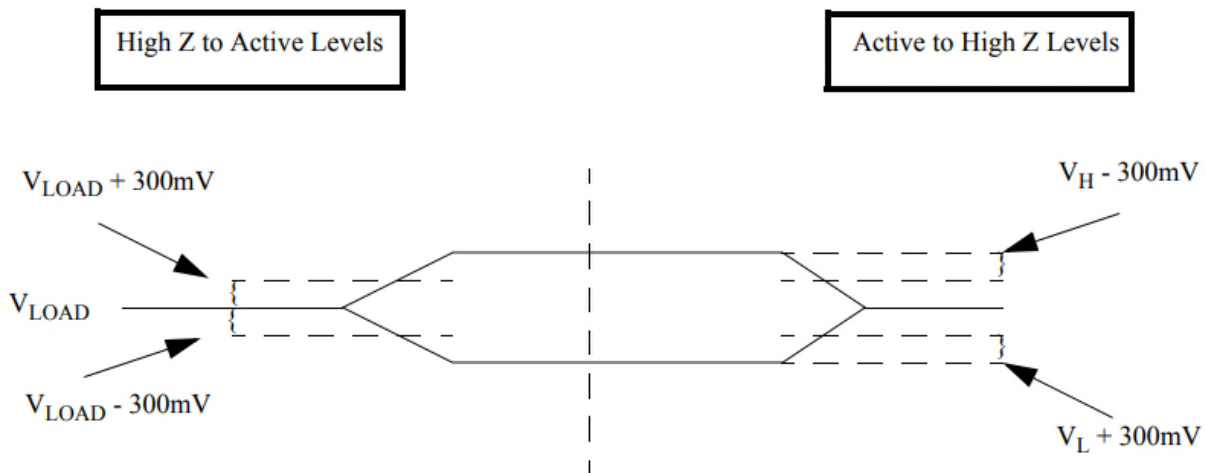
-55°C to +125°C for (C) screening ( $V_{DD} = 3.3V \pm 0.3V$ )

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{AVAV}^{1,6}$	Read cycle time	20		ns
$t_{AVSK}^5$	Address valid to address valid skew time		4	ns
$t_{AVQV}$	Read access time		20	ns
$t_{AXQX}$	Output hold time	3		ns
$t_{GLQX}$	$\bar{G}$ -controlled Output Enable time	0		ns
$t_{GLQV}$	$\bar{G}$ -controlled Output Enable time (Read Cycle 3)		10	ns
$t_{GHQZ}^2$	$\bar{G}$ -controlled output three-state time		10	ns
$t_{ETQX}^3$	$\bar{E}$ -controlled Output Enable time	3		ns
$t_{AVET2}^5$	Address setup time for read ( $\bar{E}$ -controlled)	-4		ns
$t_{ETQV}^3$	$\bar{E}$ -controlled access time		20	ns
$t_{EFQZ}^{1,2,4}$	$\bar{E}$ -controlled output three-state time		10	ns

**Notes:**

\* Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Functional test.
2. Three-state is defined as a 300mV change from steady-state output voltage (see Figure 3).
3. The ET (chip enable true) notation refers to the latter falling edge of  $\bar{E}$ . SEU immunity does not affect the read parameters.
4. The EF (chip enable false) notation refers to the latter rising edge of  $\bar{E}$ . SEU immunity does not affect the read parameters.
5. Guaranteed by design
6. Address changes prior to satisfying  $t_{AVAV}$  minimum is an invalid operation



**Figure 3. 3.3-Volt SRAM Loading**

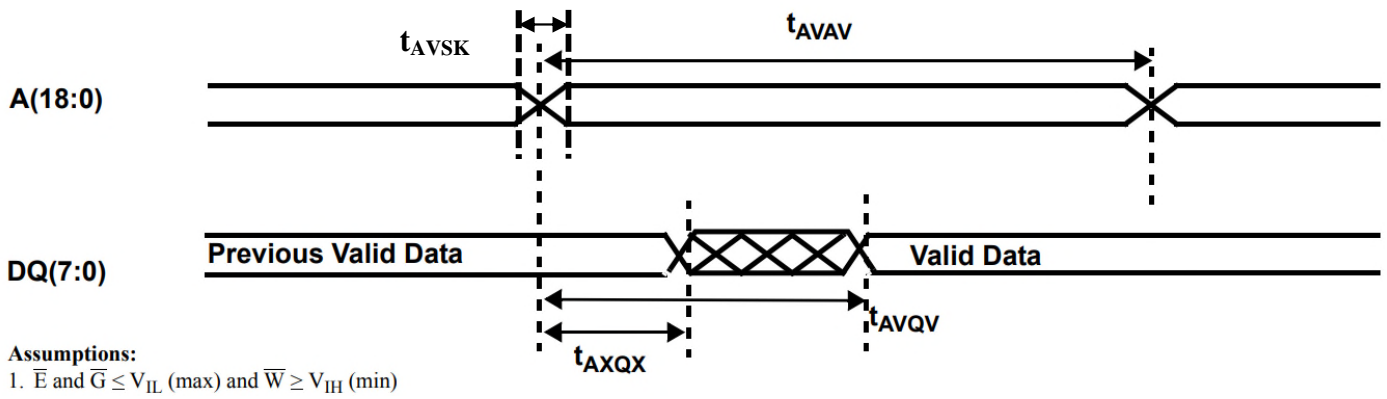
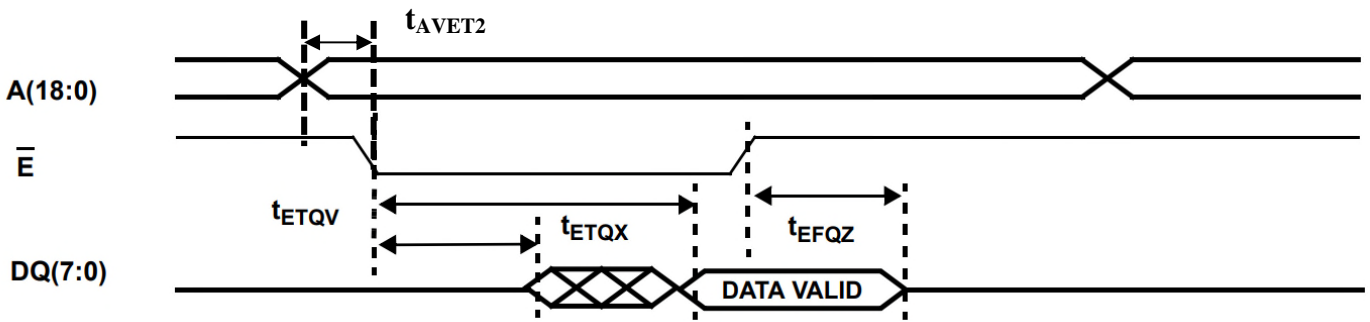
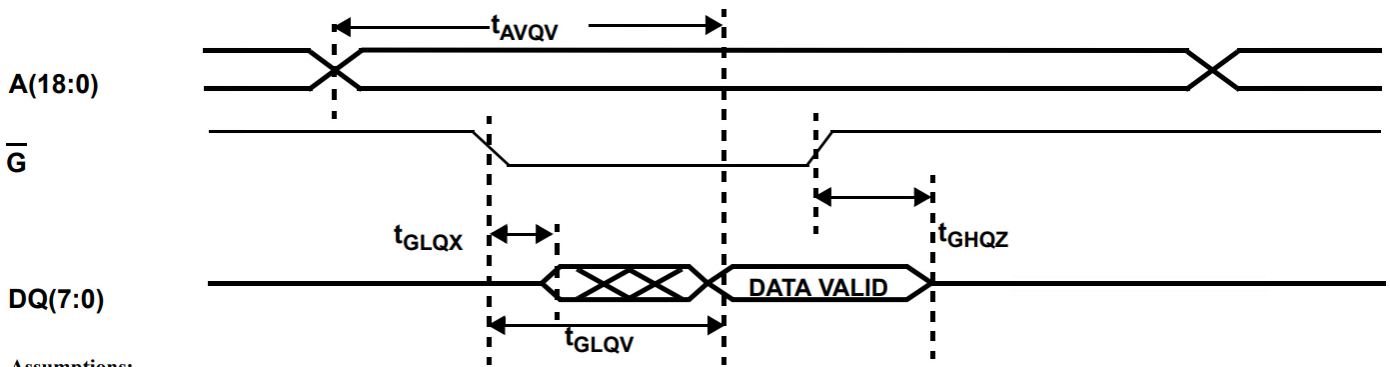


Figure 4a. SRAM Read Cycle 1: Address Access



**Assumptions:**  
 1.  $\bar{G} \leq V_{IL}$  (max) and  $\bar{W} \geq V_{IH}$  (min)

Figure 4b. SRAM Read Cycle 2: Chip Enable-Controlled Access



**Assumptions:**  
 1.  $\bar{E} \leq V_{IL}$  (max) and  $\bar{W} \geq V_{IH}$  (min)

Figure 4c. SRAM Read Cycle 3: Output Enable-Controlled Access

**AC CHARACTERISTICS WRITE CYCLE (Pre/Post-Radiation)\***-55°C to +125°C for (C) screening ( $V_{DD} = 3.3V \pm 0.3V$ )

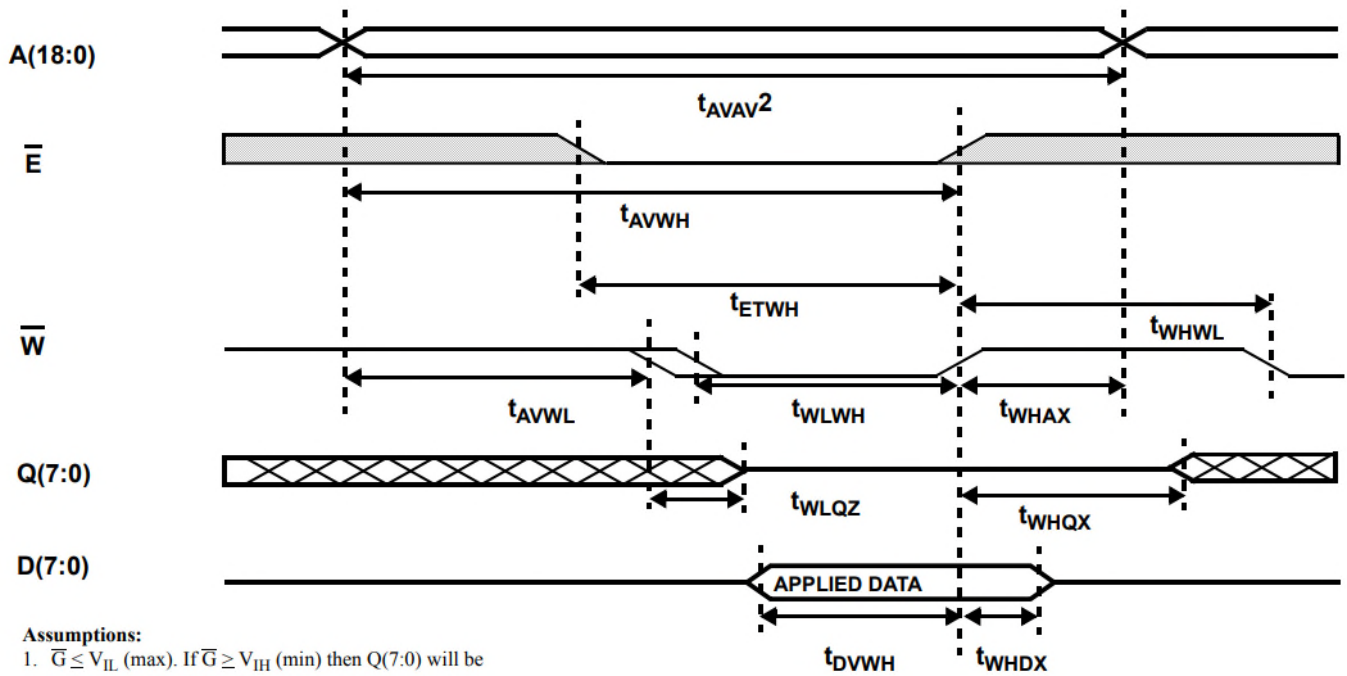
SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{AVAV}^1$	Write cycle time	20		ns
$t_{ETWH}$	Chip Enable to end of write	20		ns
$t_{AVET}$	Address setup time for write ( $\bar{E}$ - controlled)	0		ns
$t_{AVWL}$	Address setup time for write ( $\bar{W}$ - controlled)	0		ns
$t_{WLWH}$	Write pulse width	20		ns
$t_{WHAX}$	Address hold time for write ( $\bar{W}$ - controlled)	2		ns
$t_{EFAX}$	Address hold time for Chip Enable ( $\bar{E}$ - controlled)	0		ns
$t_{WLQZ}^2$	$\bar{W}$ - controlled three-state time		10	ns
$t_{WHQX}$	$\bar{W}$ - controlled Output Enable time	4		ns
$t_{ETEF}$	Chip Enable pulse width ( $\bar{E}$ - controlled)	20		ns
$t_{DVWH}$	Data setup time	15		ns
$t_{WHDX}$	Data hold time	2		ns
$t_{WLEF}$	Chip Enable controlled write pulse width	20		ns
$t_{DVEF}$	Data setup time	15		ns
$t_{EFDX}$	Data hold time	2		ns
$t_{AVWH}$	Address valid to end of write	20		ns
$t_{WHWL}^1$	Write disable time	5		ns

**Notes:**

\*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019

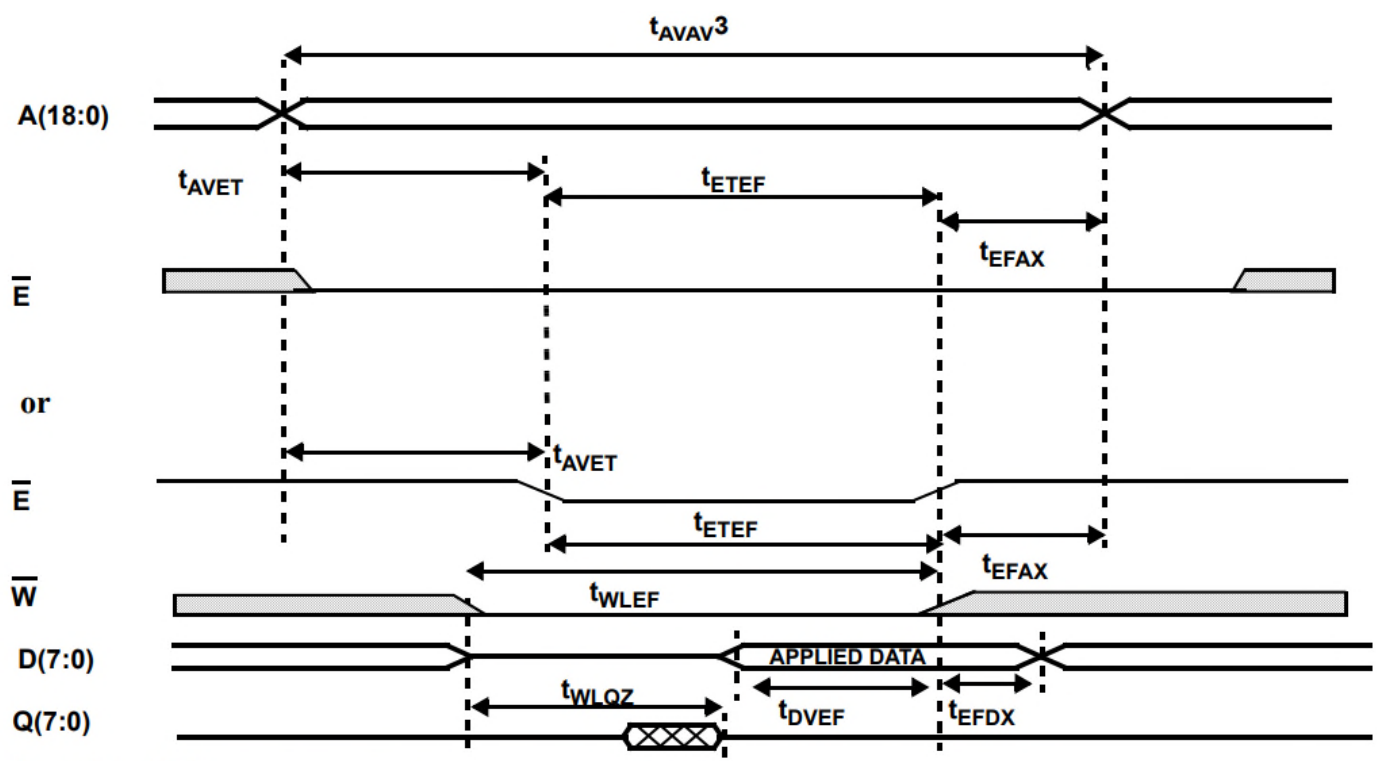
1. Functional test performed with outputs disabled ( $\bar{G}$  high).
2. Three-state is defined as 300mV change from steady-state output voltage (see Figure 3).





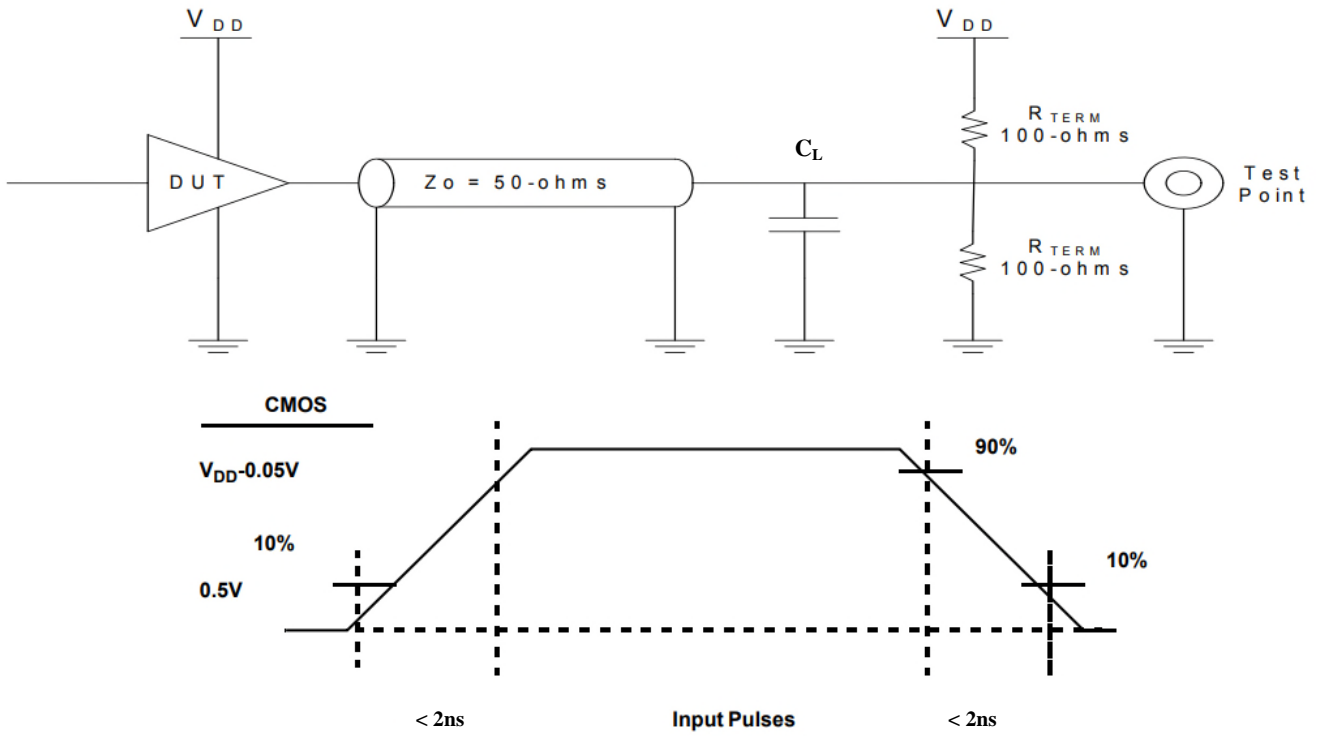
- Assumptions:**
1.  $\bar{G} \leq V_{IL}(\text{max})$ . If  $\bar{G} \geq V_{IH}(\text{min})$  then Q(7:0) will be in three-state for the entire cycle.
  2.  $\bar{G}$  high for  $t_{AVAV}$  cycle.

**Figure 5a. SRAM Write Cycle 1: Write Enable – Controlled Access**



- Assumptions & Notes:**
1.  $\bar{G} \leq V_{IL}(\text{max})$ . If  $\bar{G} \geq V_{IH}(\text{min})$  then Q(7:0) will be in three-state for the entire cycle.
  2. Either  $\bar{E}$  scenario above can occur.
  3.  $\bar{G}$  high for  $t_{AVAV}$  cycle.

**Figure 5b. SRAM Write Cycle 2: Chip Enable - Controlled Access**



**Figure 6. AC Test Loads and Input Waveforms**

**Notes:**

1. 50pF including scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input =  $V_{DD}/2$ ).

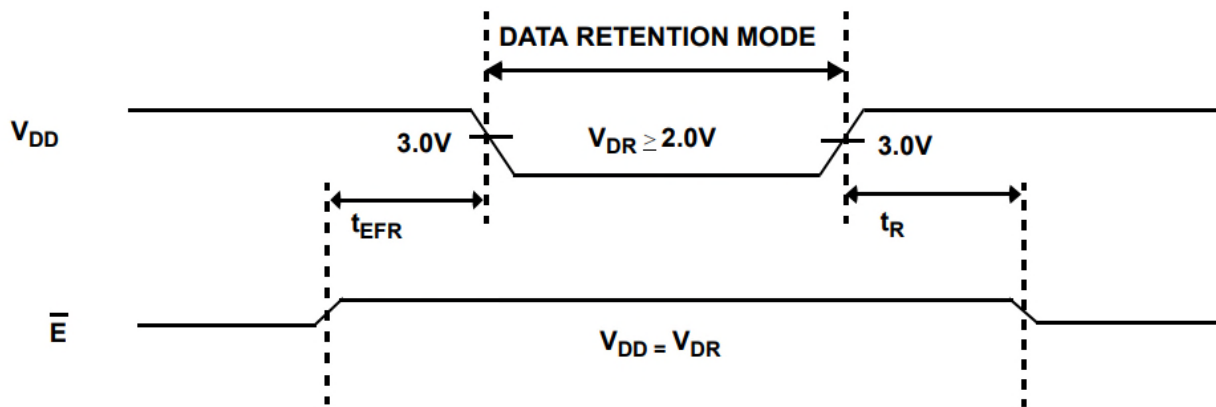


Figure 7. Low  $V_{DD}$  Data Retention Waveform

**DATA RETENTION CHARACTERISTICS (Pre-Radiation)\***

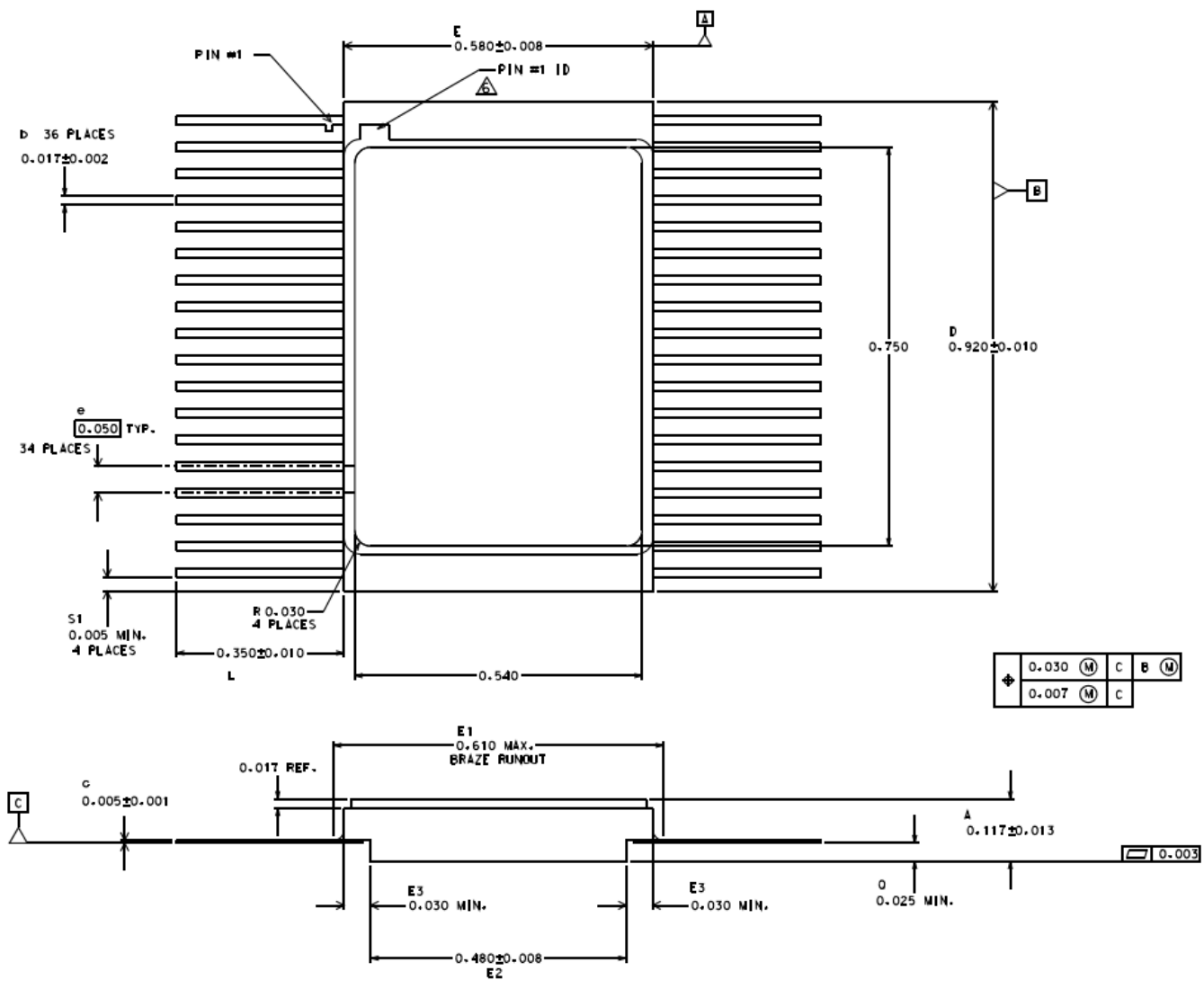
( $V_{DD} = V_{DD}(\min)$ , 1 Sec DR Pulse)

SYMBOL	PARAMETER	TEMP	MINIMUM	MAXIMUM	UNIT
$V_{DR}$	VDD for data retention	--	2.0	--	V
$I_{DDR}^1$	Data retention current	-55°C	--	16	mA
		25°C	--	16	mA
		125°C	--	45	mA
$t_{EFR}^1$	Chip Enable to data retention time	--	0	--	ns
$t_R^1$	Operation recovery time	--	$t_{AVAV}$	--	ns

**Notes:**

\* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1.  $E = V_{DR}$  all other inputs =  $V_{DR}$  or  $V_{SS}$

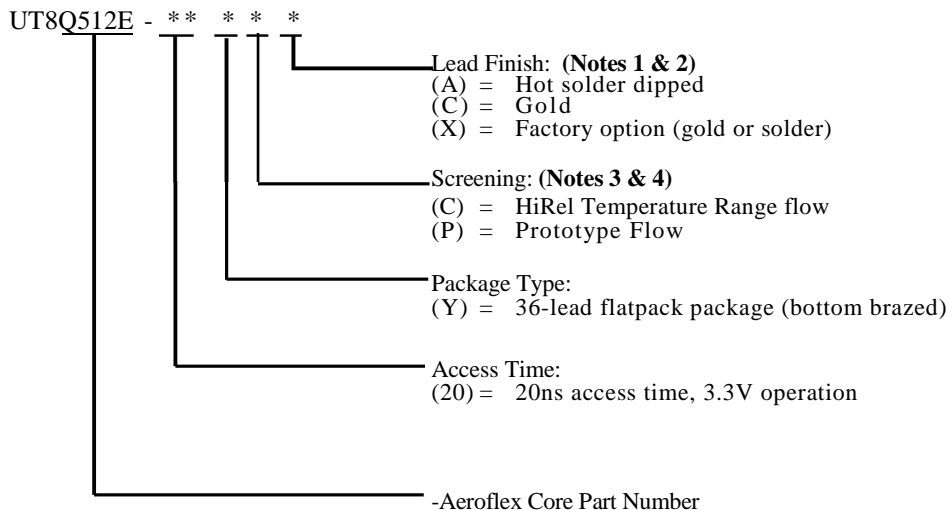


1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Dimensions are in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: no alphanumeric. One or both ID methods may be used for Pin 1 ID.
7. Letter designators are in accordance with MIL-STD-1835.
8. Dimensions shown are in inches

**Figure 8. 36-pin Ceramic FLATPACK**

## ORDERING INFORMATION

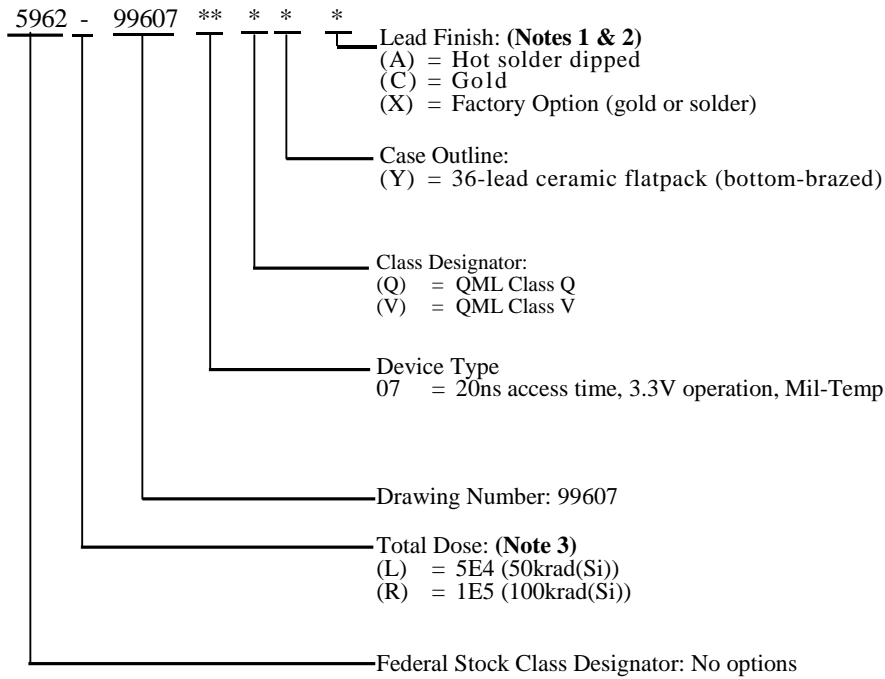
### 512K x 8 SRAM:



#### Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. HiRel Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

## 512K x 8 SRAM: SMD



### Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering.

## NOTES

### ***Cobham Semiconductor Solutions – Datasheet Definitions***

*Advanced Datasheet - Product In Development (datasheet subject to change)*

*Preliminary Datasheet – Product in Characterization and Shipping Prototypes (datasheet subject to change)*

*Datasheet – Product in Production*

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## REVISION HISTORY

Date	Revision	Change Description
July 15, 2019	A	added wording addressing read app note AN-MEM-002 and added timing parameters to AC Characteristics Read Cycle table, figure 4a and 4b; Raised max TID to 100krad; Changed max $V_{DD}$ and $V_{I/O}$ to match SMD; Removed extended industrial temp range offering; Changed electrical parameters $C_{in}$ , $C_{IO}$ , $V_{OH1}$ , $V_{OH2}$ , and $I_{DD}(SB)$ due to performance changes in new die revision; Corrected typos
June 2020	B	Raised max TID to 100krad; changed SEU onset LET; added SEL to table 2; changed abs max VDD and VI/O to match SMD; removed extended industrial temp range part offering; changed input capacitance and bidirectional I/O capacitance to 14 and 16 pF respectively; changed standby current and IDDR to 16mA; Revised tGLQX and tWHAX timing; revised figure 6 to match SMD