Functional Overview

The STAR III product line presently consist of three standard types of Militarized VMEbus based Single Board Computer boards. The first is called the Input Output Processor (IOP) and the second is called the Central Processor Module (CPM). Both STAR III boards make use of the R4430PC MIPS RISC Processor operating at 50 MHZ (100 MHZ internal, cycle time 10ns) and utilizing the VxWorks Real Time Operating System (RTOS). The processor is rated at 60 VAX MIPS and 33 MFLOP/sec for floating point calculations. The third is very similar to the CPM mentioned above but utilizes the R4700 RISC Processor for greater performance.

Each VMEbus card (IEEE 1014, 6U 160 Form Factor) contains the following:
- Processor L1 Cache for Instructions and Data (16KBytes each)
- Address space 64 Gigabytes in 64-Bit mode, 4 Gigabytes in 32-Bit mode
- Dram 64/16 MBytes CPM/IOP, with error detection & correction
- Flash 16/48 MBytes CPM/IOP
- NVRam 8KBytes
- Four 32 bit programmable Timers
- Real Time Clock (RTC), with battery backup capabilities
- DMA Controller
- VMEbus Full Master/Slave D8, D16, D32, D64, A24, A32, up to 58MB/second
- Two Independent RS-232 Ports
- One Ethernet AUI Port IEEE 802.3 Compatible
- As many as Three (3) 1553B Ports on IOP only, Supports DDC BU-61580 as RT, BM and BC
- Mezzanine expansion connector
- Two Diagnostic Leds
- Supports Numerous Exception Interrupts and 25 Hardware Interrupts
- PMON Built in Test
Daughter Card Options
through use of
Mezzanine Connector
available for
growth

Virtual local Bus - 0 and Local Bus - 1

32-Bit
DMA
Controller

R4300/ R4700

32-Bit
Timers

SE BUS (200MB/sec)

LED

INTERRUPT

DRAM

Controller

16K Byte
I-Cache

16K Byte
D-Cache

Integer
Unit

Floating
Point
Unit

CPU

Interrupt
Controller

RAID0 Interface
Controller

Floating Point

Controller

EDC

Generate

EDC

Correct

Interrupt
Controller

R4000

Interface
Controller

VMEBUS

Arbitor

VMEBUS

Controller

DMA

Controller

Output
PIPE

Input
PIPE

Turbo
Channel
Controller

32-Bit
Timers

UART & Enet (via P2)

1553B Interface (via P2)

Mezzanine Connector

Expansion Port
100MB/sec

Reg Buff

Reg Buff

Reg Buff

Power Supply Shut-Down
Signature Resistors

Daughter-Card Discretes
• Power-Supply-Off/Down
• Watch-De-OX/Execute & Fail
• Slot Identification

1553 Control

1553 Control

1553 Control

1553 Control

Real
Clock

Time

UART

Ethernet

Controller

1553

Control

LED

Control

Mem / Clk

Control

Addr / Ctrl

Decoder

1553

Control

Xilinx

FPGA

A

Buffer

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Specifications

Power ............................................. 15W
Voltage Requirements .............. +5V@ 3A max, +12V@ 150mA max
Operating Temperature .............. Rail Temperature, -54°C to +55°C (cont.), -54°C to +71°C (Intermittent)
Storage Temperature ................. -54°C to +125°C
Relative Humidity ...................... Up to 95% non-condensing
Altitude Operating & shipping ...... 50,000 feet
Acceleration ................................. 12G
Random Vibration ....................... 15 Hz to 2KHz @ .01g^2/Hz
Shock ............................................ 20G for 11 seconds
Physical Form Factor .................. Double-sided VME 6U-160
Dimensions Height ....................... 9.2 inches (233mm)
                          Depth ....................... 6.3 inches (160mm)
                          Thickness ............. .8 inches (20mm)
Weight .......................................... 1.865 pounds
Cooling ........................................ Conductive

R4X00 MIPS Processor Description
The MIPS R4X00 utilizes a RISC type architecture to provide the latest state of the art processor engine, below is a list of attributes provided by this processor. A serial PROM is used to set up and initialize the processor prior to startup.

♦ 50MHz external clock, 100MHz internal clock with 10ns cycle time.
♦ Thirty-two 64-Bit registers
♦ Physical Address Space: 4 Gbytes 32-Bit mode / 64 Gbytes 64-Bit mode
♦ Dynamically configurable big/little endian
♦ Floating Point Unit Single & Double precision operations
♦ 16Kbyte Instruction cache
♦ 16Kbyte write back Data cache
♦ Memory Management, Translation Lookaside Buffer (TLB) for fast logical to physical address translation
Ordering Information

STAR III R4430 RISC Processor Boards

ACT 8010 - 16 - 16 - 3
RAM Size  Flash Size  1553 Port

0 – None
1 – 1 Port
2 – 2 Port
3 – 3 Port

16 – 16 Mbytes
32 – 32 Mbytes
48 – 48 Mbytes
64 – 64 Mbytes

16 – 16 Mbytes
64 – 64 Mbytes

Standard Part Offering
CPM = ACT 8010-64-48-0
IOP = ACT 8010-16-16-2

Note: ACT 8011 Series STAR III Boards utilize the R4700 RISC Processor and has the same part numbering scheme as the ACT 8010.

Specifications subject to change without notice