FEATURES

- 1.2μ CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 14-pin DIP
  - 14-lead flatpack
- UT54ACS74 - SMD 5962-96534
- UT54ACTS74 - SMD 5962-96535

DESCRIPTION

The UT54ACS74 and the UT54ACTS74 contain two independent D-type positive triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirement is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The devices are characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

<table>
<thead>
<tr>
<th>PRE</th>
<th>CLR</th>
<th>CLK</th>
<th>D</th>
<th>Q</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>↑</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>Q_o</td>
<td>Q_o</td>
</tr>
</tbody>
</table>

Note:
1. The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. In addition, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

PINOUTS

14-Pin DIP

<table>
<thead>
<tr>
<th>CLR1</th>
<th>D1</th>
<th>CLK1</th>
<th>PRE1</th>
<th>Q1</th>
<th>Q1</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>6</td>
</tr>
</tbody>
</table>

14-Lead Flatpack

<table>
<thead>
<tr>
<th>CLR1</th>
<th>D1</th>
<th>CLK1</th>
<th>PRE1</th>
<th>Q1</th>
<th>Q1</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>6</td>
</tr>
</tbody>
</table>

LOGIC SYMBOL

Note:
OPERATIONAL ENVIRONMENT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose</td>
<td>1.0E6</td>
<td>rads(Si)</td>
</tr>
<tr>
<td>SEU Threshold</td>
<td>80</td>
<td>MeV-cm²/mg</td>
</tr>
<tr>
<td>SEL Threshold</td>
<td>120</td>
<td>MeV-cm²/mg</td>
</tr>
<tr>
<td>Neutron Fluence</td>
<td>1.0E14</td>
<td>n/cm²</td>
</tr>
</tbody>
</table>

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td>-0.3 to 7.0</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>Voltage any pin</td>
<td>-.3 to VDD +.3</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature range</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Maximum junction temperature</td>
<td>+175</td>
<td>°C</td>
</tr>
<tr>
<td>TLS</td>
<td>Lead temperature (soldering 5 seconds)</td>
<td>+300</td>
<td>°C</td>
</tr>
<tr>
<td>ΘJC</td>
<td>Thermal resistance junction to case</td>
<td>20</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ii</td>
<td>DC input current</td>
<td>±10</td>
<td>mA</td>
</tr>
<tr>
<td>PD</td>
<td>Maximum power dissipation</td>
<td>1</td>
<td>W</td>
</tr>
</tbody>
</table>

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td>4.5 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage any pin</td>
<td>0 to VDD</td>
<td>V</td>
</tr>
<tr>
<td>TC</td>
<td>Temperature range</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>
**DC ELECTRICAL CHARACTERISTICS**

(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V; -55°C < T<sub>C</sub> < +125°C); Unless otherwise noted, T<sub>C</sub> is per the temperature range ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Low-level input voltage&lt;sup&gt;1&lt;/sup&gt;</td>
<td>ACTS&lt;br&gt;ACS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>High-level input voltage&lt;sup&gt;1&lt;/sup&gt;</td>
<td>ACTS&lt;br&gt;ACS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input leakage current&lt;sup&gt;1&lt;/sup&gt;</td>
<td>ACTS/ACS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Low-level output voltage&lt;sup&gt;3&lt;/sup&gt;</td>
<td>ACTS&lt;br&gt;ACS</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>High-level output voltage&lt;sup&gt;3&lt;/sup&gt;</td>
<td>ACTS&lt;br&gt;ACS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Short-circuit output current&lt;sup&gt;2, 4&lt;/sup&gt;</td>
<td>ACTS/ACS</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Output current&lt;sup&gt;10&lt;/sup&gt; (Sink)</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt; or V&lt;sub&gt;SS&lt;/sub&gt;&lt;br&gt;V&lt;sub&gt;OL&lt;/sub&gt; = 0.4V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>Output current&lt;sup&gt;10&lt;/sup&gt; (Source)</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt; or V&lt;sub&gt;SS&lt;/sub&gt;&lt;br&gt;V&lt;sub&gt;OH&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt; - 0.4V</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P&lt;sub&gt;total&lt;/sub&gt;</td>
<td>Power dissipation&lt;sup&gt;2, 8, 9&lt;/sup&gt;</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50pF</td>
<td>1.9</td>
<td>mW/ MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;DDQ&lt;/sub&gt;</td>
<td>Quiescent Supply Current</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.5V</td>
<td>10</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔI&lt;sub&gt;DDQ&lt;/sub&gt;</td>
<td>Quiescent Supply Current Delta</td>
<td>For input under test&lt;br&gt;V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt; - 2.1V&lt;br&gt;For all other inputs&lt;br&gt;V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt; or V&lt;sub&gt;SS&lt;/sub&gt;&lt;br&gt;V&lt;sub&gt;DD&lt;/sub&gt; = 5.5V</td>
<td>1.6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input capacitance&lt;sup&gt;5&lt;/sup&gt;</td>
<td>f = 1MHz @ 0V</td>
<td>15</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Output capacitance&lt;sup&gt;5&lt;/sup&gt;</td>
<td>f = 1MHz @ 0V</td>
<td>15</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>
Notes:
1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\text{min}) + 20\%, -0\%$; $V_{IL} = V_{IL}(\text{max}) + 0\%, -50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm$^2$, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and $V_{SS}$ at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose $\leq 1E6$ rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.
AC ELECTRICAL CHARACTERISTICS 2
(VDD = 5.0V ±10%; VSS = 0V; -55°C < Tc < +125°C); Unless otherwise noted, Tc is per the temperature range ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPHL</td>
<td>CLK to Q, Q̄</td>
<td>3</td>
<td>21</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>CLK to Q, Q̄</td>
<td>1</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>PRE to Q</td>
<td>1</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>tPHL</td>
<td>PRE to Q̄</td>
<td>3</td>
<td>19</td>
<td>ns</td>
</tr>
<tr>
<td>tPHL</td>
<td>CLR to Q</td>
<td>3</td>
<td>19</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>CLR to Q̄</td>
<td>1</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>fMAX</td>
<td>Maximum clock frequency</td>
<td></td>
<td>71</td>
<td>MHz</td>
</tr>
<tr>
<td>tSU1</td>
<td>PRE or CLR inactive</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSU2</td>
<td>Setup time before CLK ↑</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tH</td>
<td>Data hold time after CLK ↑</td>
<td>2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tW</td>
<td>Minimum pulse width</td>
<td></td>
<td>7</td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Based on characterization, hold time (tH) of 0ns can be assumed if data setup time (tSU2) is ≥10ns. This is guaranteed, but not tested.
FLATPACK PACKAGES

DIMENSION SYMBOLS

- A
- D
- E
- E1
- E2
- E3
- L
- L1
- L2
- S1
- S2
- S3

LEAD COUNT

- 14
- 16

PACKAGE CONFIG

- -03
- -04
- -05
Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
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