FEATURES
- AND-gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Direct clear
- 1.2μ CMOS (ACTS) and 0.6μ CRH CMOS (ACS)
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 14-pin DIP (ACTS only)
  - 14-lead flatpack
- UT54ACS164 - SMD 5962-96556
- UT54ACTS164 - SMD 5962-96557

DESCRIPTION
The UT54ACS164 and the UT54ACTS164 are 8-bit shift registers which feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high-level at both serial inputs sets the first flip-flop to the high level at the next clock pulse. Data at the serial inputs may be changed while the clock is high or low, providing the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

The devices are characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CLK</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
</tr>
</tbody>
</table>

Notes:
1. QA0, QB0, QH0 = the level of QA, QB or QH, respectively, before the indicated steady-state input conditions were established.
2. QA0 and QGn = the level of QA or QG before the most recent ↑ transition of the clock; indicates a one-bit shift.

PINOUTS

LOGIC SYMBOL

Note:
### OPERATIONAL ENVIRONMENT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose</td>
<td>1.0E6 (ACTS) 500K (ACS)</td>
<td>rads(Si)</td>
</tr>
<tr>
<td>SEU Threshold</td>
<td>80</td>
<td>MeV-cm²/mg</td>
</tr>
<tr>
<td>SEL Threshold</td>
<td>120</td>
<td>MeV-cm²/mg</td>
</tr>
<tr>
<td>Neutron Fluence</td>
<td>1.0E14</td>
<td>n/cm²</td>
</tr>
</tbody>
</table>

**Notes:**
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td>-0.3 to 7.0</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>Voltage any pin</td>
<td>-0.3 to VDD + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature range</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Maximum junction temperature</td>
<td>+175</td>
<td>°C</td>
</tr>
<tr>
<td>TLS</td>
<td>Lead temperature (soldering 5 seconds)</td>
<td>+300</td>
<td>°C</td>
</tr>
<tr>
<td>$\Theta_{JC}$</td>
<td>Thermal resistance junction to case</td>
<td>15.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ii</td>
<td>DC input current</td>
<td>±10</td>
<td>mA</td>
</tr>
<tr>
<td>PD</td>
<td>Maximum power dissipation</td>
<td>1</td>
<td>W</td>
</tr>
</tbody>
</table>

**Note:**
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td>4.5 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage any pin</td>
<td>0 to VDD</td>
<td>V</td>
</tr>
<tr>
<td>TC</td>
<td>Temperature range</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>
DC ELECTRICAL CHARACTERISTICS

(VDD = 5.0V ±10%; VSS = 0V; -55°C < TC < +125°C); Unless otherwise noted, Tc is per the temperature range ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
</table>
| VIL    | Low-level input voltage 1 | ACTS
ACS | 0.8 | .3VDD |
| VIL    | High-level input voltage 1 | ACTS
ACS | .5VDD | .7VDD |
| IIN    | Input leakage current | ACTS/ACS | VIN = VDD or VSS | -1 | 1 μA |
| VIL    | Low-level output voltage 3 | ACTS
ACS | IOL = 8.0mA | 0.40 |
| VIL    | High-level output voltage 3 | ACTS
ACS | IOH = -8.0mA | .7VDD |
| IOS    | Short-circuit output current 2,4 | ACTS/ACS | VO = VDD and VSS | -200 | 200 mA |
| IOL    | Output current 10 | (Sink) | VIN = VDD or VSS
VOL = 0.4V | 8 | mA |
| IOH    | Output current 10 | (Source) | VIN = VDD or VSS
VOH = VDD - 0.4V | -8 | mA |
| Ptotal | Power dissipation 2, 8, 9 | C_L = 50pF | 1.9 | mW/ MHz |
| IDDQ   | Quiescent Supply Current | Pre-Rad
Post-Rad
Device Type 01 | VIN = VDD or VSS
VDD = VDD MAX | 10 | μA |
| ΔIDDQ  | Quiescent Supply Current Delta | ACTS | For input under test
For all other inputs | VIN = VDD - 2.1V
VIN = VDD or VSS
VDD = 5.5V | 1.6 | mA |
| CIN    | Input capacitance 5 | f = 1MHz @ 0V | 15 | pF |
| COUT   | Output capacitance 5 | f = 1MHz @ 0V | 15 | pF |
Notes:
1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: \( V_{IH} = V_{IH\text{min}} + 20\% \) to \( -0\% \); \( V_{IL} = V_{IL\text{max}} + 0\% \) to \( -50\% \), as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to \( V_{IH\text{min}} \) and \( V_{IL\text{max}} \).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density \( \leq 5.0E5 \text{ amps/cm}^2 \), the maximum product of load capacitance (per output buffer) times frequency should not exceed \( 3,765 \text{ pF/MHz} \).
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and \( V_{SS} \) at frequency of \( 1\text{MHz} \) and a signal amplitude of \( 50\text{mV rms} \) maximum.
6. Maximum allowable relative shift equals \( 50\text{mV} \).
7. Device type 01 is only offered with a TID tolerance guarantee of \( 1E6 \text{ rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si)} \), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.
AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V \pm 10\%; V_{SS} = 0V \text{^1}, -55^\circ C < T_C < +125^\circ C); Unless otherwise noted, T_c is per the temperature range ordered.

\begin{center}
\begin{tabular}{|c|c|c|c|}
\hline
\textbf{SYMBOL} & \textbf{PARAMETER} & \textbf{MINIMUM} & \textbf{MAXIMUM} \\
\hline
\text{t}_{\text{PHL}} & CLK to Qn & 4 & 21 \\
\hline
\text{t}_{\text{PLH}} & CLK to Qn & 2 & 18 \\
\hline
\text{t}_{\text{PHL}} & CLR to Qn & 5 & 21 \\
\hline
\text{f}_{\text{MAX}} & Maximum clock frequency & & 83 MHz \\
\hline
\text{t}_{\text{SU1}} & CLR inactive
Setup time before CLK \uparrow & 4 & ns \\
\hline
\text{t}_{\text{SU2}} & Data setup time before CLK\uparrow & 4 & ns \\
\hline
\text{t}_H^3 & Data hold time after CLK \uparrow & 2 & ns \\
\hline
\text{t}_W & Minimum pulse width
CLR low
CLK high
CLK low & 6 & ns \\
\hline
\end{tabular}
\end{center}

Notes:

1. Maximum allowable relative shift equals 50mV.
2. Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
3. Based on characterization, hold time (t_H) of 0ns can be assumed if data setup time (t_{SU2}) is \geq 10ns. This is guaranteed, but not tested.
Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
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DATA SHEET REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
<th>Author</th>
</tr>
</thead>
<tbody>
<tr>
<td>10-17</td>
<td>Page 4 edited IDDQ</td>
<td>RT</td>
</tr>
<tr>
<td></td>
<td>Applied new Cobham Data Sheet template to the document.</td>
<td></td>
</tr>
<tr>
<td>1-18</td>
<td>Updates to reflect current SMD</td>
<td>RT</td>
</tr>
</tbody>
</table>