# Standard Products

## UT54ACS10/UT54ACTS10

### Triple 3-Input NAND Gates

Datasheet  
November 2010  
www.aeroflex.com/logic

### FEATURES
- 1.2μ CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 14-pin DIP
  - 14-lead flatpack
- UT54ACS10 - SMD 5962-96520
- UT54ACTS10 - SMD 5962-96521

### DESCRIPTION
The UT54ACS10 and the UT54ACTS10 are triple three-input NAND gates. The circuits perform the Boolean functions $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The devices are characterized over full military temperature range of -55°C to +125°C.

### FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

### LOGIC SYMBOL

```
A1
B1
C1
A2
B2
C2
A3
B3
C3
```

\[
Y_1 \quad \& \quad Y_2 \quad \rightarrow \quad Y_3
\]

### PINOUTS

#### 14-Pin DIP

```
A1 | 1 | 14 | VDD
B1 | 2 | 13 | C1
A2 | 3 | 12 | Y1
B2 | 4 | 11 | C3
C2 | 5 | 10 | B3
Y2 | 6 | 9  | A3
VSS| 7 | 8  | Y3
```

#### 14-Lead Flatpack

```
A1 | 1 | 14 | VDD
B1 | 2 | 13 | C1
A2 | 3 | 12 | Y1
B2 | 4 | 11 | C3
C2 | 5 | 10 | B3
Y2 | 6 | 9  | A3
VSS| 7 | 8  | Y3
```

### LOGIC DIAGRAM

```
A1
B1
C1

\[ \rightarrow \]

Y1
```

```
A2
B2
C2

\[ \rightarrow \]

Y2
```

```
A3
B3
C3

\[ \rightarrow \]

Y3
```

### Note:
OPERATIONAL ENVIRONMENT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose</td>
<td>1.0E6</td>
<td>rads(Si)</td>
</tr>
<tr>
<td>SEU Threshold²</td>
<td>80</td>
<td>MeV·cm²/mg</td>
</tr>
<tr>
<td>SEL Threshold</td>
<td>120</td>
<td>MeV·cm²/mg</td>
</tr>
<tr>
<td>Neutron Fluence</td>
<td>1.0E14</td>
<td>n/cm²</td>
</tr>
</tbody>
</table>

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td>-0.3 to 7.0</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Voltage any pin</td>
<td>-.3 to VDD +.3</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature range</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Maximum junction temperature</td>
<td>+175</td>
<td>°C</td>
</tr>
<tr>
<td>TLP</td>
<td>Lead temperature (soldering 5 seconds)</td>
<td>+300</td>
<td>°C</td>
</tr>
<tr>
<td>ΘJC</td>
<td>Thermal resistance junction to case</td>
<td>20</td>
<td>°C/W</td>
</tr>
<tr>
<td>II</td>
<td>DC input current</td>
<td>±10</td>
<td>mA</td>
</tr>
<tr>
<td>PD</td>
<td>Maximum power dissipation</td>
<td>1</td>
<td>W</td>
</tr>
</tbody>
</table>

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td>4.5 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage any pin</td>
<td>0 to VDD</td>
<td>V</td>
</tr>
<tr>
<td>TC</td>
<td>Temperature range</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>
**DC ELECTRICAL CHARACTERISTICS**

\((V_{DD} = 5.0V \pm 10\%; V_{SS} = 0V, -55^\circ C < T_C < +125^\circ C)\); Unless otherwise noted, \(T_c\) is per the temperature range ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IL})</td>
<td>Low-level input voltage (^1)</td>
<td>(V_{IN} = V_{DD} ) or (V_{SS})</td>
<td>0.8 (V_{DD})</td>
<td>.3 (V_{DD})</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>High-level input voltage (^1)</td>
<td>(I_{OL} = 8.0mA)</td>
<td>.5 (V_{DD})</td>
<td>.7 (V_{DD})</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IN})</td>
<td>Input leakage current</td>
<td>(V_{IN} = V_{DD} ) or (V_{SS})</td>
<td>-1 (\mu A)</td>
<td>1 (\mu A)</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Low-level output voltage (^3)</td>
<td>(I_{OL} = 100\mu A)</td>
<td>0.40 (V)</td>
<td>0.25 (V)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>High-level output voltage (^3)</td>
<td>(I_{OH} = -8.0mA)</td>
<td>.7 (V_{DD})</td>
<td>(V_{DD} - 0.25)</td>
<td>V</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Short-circuit output current (^2),(^4)</td>
<td>(V_O = V_{DD} ) and (V_{SS})</td>
<td>-200 mA</td>
<td>200 mA</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td>Output current (^10) (Sink)</td>
<td>(V_{IN} = V_{DD} ) or (V_{SS})</td>
<td>8 (mA)</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(I_{OH})</td>
<td>Output current (^10) (Source)</td>
<td>(V_{IN} = V_{DD} ) or (V_{SS})</td>
<td>-8 (mA)</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(P_{total})</td>
<td>Power dissipation (^2),(^8),(^9)</td>
<td>(C_L = 50pF)</td>
<td>1.8 mW/MHz</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(I_{DDQ})</td>
<td>Quiescent Supply Current</td>
<td>(V_{DD} = 5.5V)</td>
<td>10 (\mu A)</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(\Delta I_{DDQ})</td>
<td>Quiescent Supply Current Delta</td>
<td>For input under test (V_{IN} = V_{DD} - 2.1V)</td>
<td>1.6 mA</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(C_{IN})</td>
<td>Input capacitance (^5)</td>
<td>(f = 1MHz \oplus 0V)</td>
<td>15 pF</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(C_{OUT})</td>
<td>Output capacitance (^5)</td>
<td>(f = 1MHz \oplus 0V)</td>
<td>15 pF</td>
<td>(\mu A)</td>
<td></td>
</tr>
</tbody>
</table>
Notes:
1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\text{min}) + 20\%$, - 0%; $V_{IL} = V_{IL}(\text{max}) + 0\%$, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and $V_{SS}$ at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose $\leq 1E6$ rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.
AC ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V 1, -55°C < T<sub>C</sub> < +125°C); Unless otherwise noted, T<sub>C</sub> is per the temperature range ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;PHL&lt;/sub&gt;</td>
<td>Input to Yn</td>
<td>1</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PLH&lt;/sub&gt;</td>
<td>Input to Yn</td>
<td>1</td>
<td>12</td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
### Flatpack Packages

#### Top View

- **Pin #1 ID Mark**
- **(N-2) Places**
- **(N) Places**
- **B, D, H-A-B, C, D**

#### Front View

- **L**
- **E1**
- **E2**
- **E3**

### Dimension Symbols

<table>
<thead>
<tr>
<th>PKG CONFIG</th>
<th>LEAD COUNT</th>
<th>MIL-STD 1835 DWG CONF</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>E1</th>
<th>E2</th>
<th>E3</th>
<th>e</th>
<th>k</th>
<th>L</th>
<th>O</th>
<th>S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>-03</td>
<td>14</td>
<td>F-2A</td>
<td>0.115</td>
<td>0.022</td>
<td>0.009</td>
<td>0.390</td>
<td>0.260</td>
<td>0.290</td>
<td>-----</td>
<td>-----</td>
<td>0.050</td>
<td>0.015</td>
<td>0.370</td>
<td>0.045</td>
<td>-----</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.045</td>
<td>0.015</td>
<td>0.004</td>
<td>-----</td>
<td>0.235</td>
<td>-----</td>
<td>0.130</td>
<td>0.030</td>
<td>BSC</td>
<td>0.008</td>
<td>0.270</td>
<td>0.026</td>
<td>0.005</td>
</tr>
<tr>
<td>-04</td>
<td>16</td>
<td>F-5A</td>
<td>0.115</td>
<td>0.022</td>
<td>0.009</td>
<td>0.440</td>
<td>0.285</td>
<td>0.315</td>
<td>-----</td>
<td>-----</td>
<td>0.050</td>
<td>0.015</td>
<td>0.370</td>
<td>0.045</td>
<td>-----</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.045</td>
<td>0.015</td>
<td>0.004</td>
<td>-----</td>
<td>0.245</td>
<td>-----</td>
<td>0.130</td>
<td>0.030</td>
<td>BSC</td>
<td>0.008</td>
<td>0.250</td>
<td>0.026</td>
<td>0.005</td>
</tr>
<tr>
<td>-05</td>
<td>20</td>
<td>F-9A</td>
<td>0.115</td>
<td>0.022</td>
<td>0.009</td>
<td>0.540</td>
<td>0.300</td>
<td>0.330</td>
<td>-----</td>
<td>-----</td>
<td>0.050</td>
<td>0.015</td>
<td>0.370</td>
<td>0.045</td>
<td>-----</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.045</td>
<td>0.015</td>
<td>0.004</td>
<td>-----</td>
<td>0.245</td>
<td>-----</td>
<td>0.130</td>
<td>0.030</td>
<td>BSC</td>
<td>0.008</td>
<td>0.250</td>
<td>0.026</td>
<td>0.000</td>
</tr>
</tbody>
</table>
UT54ACS10/UT54ACTS10: SMD

Lead Finish: (Notes 1 & 2)
A = Solder
C = Gold
X = Optional

Package Type:
X = 14-lead ceramic bottom-brazed dual-in-line Flatpack
C = 14-lead ceramic side-brazed dip

Class Designator:
Q = QML Class Q
V = QML Class V

Device Type:
01

Drawing Number:
96520 = UT54ACS10
96521 = UT54ACTS10

Total Dose: (Notes 3 & 4)
R = 1E5 rads(Si)
F = 3E5 rads(Si)
G = 5E5 rads(Si)
H = 1E6 rads(Si)

Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development
Preliminary Datasheet - Shipping Prototype
Datasheet - Shipping QML & Reduced Hi-Rel

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