FEATURES

- Fully populated board ready for media and AC electrical performance testing of the UT54LVDS031 and UT54LVDS032 (5V and 3V products)
- UT54LVDS031 and UT54LVDS032 attributes
  - 5V operation
    - >155.5 Mbps (77.7MHz) switching rates
  - 3V operation
    - >400 Mbps (200MHz) switching rates
  - Compatible with IEEE 1596.3SCI LVDS
  - Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard
- Ideal for testing jitter, eye-diagrams, signal integrity, etc
- 100 mil header for simple cable connection using twisted pair cable
- SMB connectors for simple connection to external test equipment
- Oscilloscope probe test points
- Prototype area provided for simple tests

INTRODUCTION

To provide a quick and easy environment to evaluate the UT54LVDS031 and UT54LVDS032 LVDS products, UTMC announces the introduction of the UT54LVDS-EVB Evaluation Board. The board supports the measurement of signal integrity over different media, bus configuration, and data toggle rates. The UT54LVDS-EVB Evaluation Board provides a simple means to evaluate the line driving capability of the UT54LVDS031 across a PCB trace and a variable length of twisted pair cable.

The board contains the UT54LVDS031 Quad Driver and the UT54LVDS032 Quad Receiver connected to allow individual line driver and receiver testing. Inputs to the UT54LVDS031 and outputs from the UT54LVDS032 are available through SMB connectors for ease of applying signals and taking measurements. Oscilloscope probe test points are available on the outputs of the driver and input to the receiver as well as the receiver outputs. A prototype area allows the user to interface the board to other circuitry in support of system evaluation.

Figure 1. UT54LVDS-EVB Evaluation Board
TEST CASES

LVDS Test 1: Variable cable Length (JP1 to JP6)

This test connects Driver 1 to Receiver 4 via a cable interconnect. SMB connector J1 is provided to connect a signal generator to the input of Driver 1. The Driver input J1 is terminated with a 50 ohm resistor. Test point 1 is provided to monitor the input signal. Test points 2+ and 3- are located on the output of Driver 1. Test points 14+ and 15- are located on the inputs of Receiver 4. SMB connector J10 and test point 13 are located on the output of Receiver 4. A PCB option for a series 450 ohm resistor (R20) is also provided in case 50 ohm probes are employed on the receiver output signal.

LVDS Test 2: Variable cable Length (JP1 to JP6)

This test connects Driver 2 to Receiver 3 via a cable interconnect. SMB connector J2 is provided to connect a signal generator to the input of Driver 2. The Driver input J2 is terminated with a 50 ohm resistor. Test point 7 is provided to monitor the input signal. Test points 6+ and 5- are located on the output of Driver 2. Test points 10+ and 9- are located on the inputs of Receiver 3. SMB connector J9 and test point 11 are located on the output of Receiver 4. A PCB option for a series 450 ohm resistor (R14) is also provided in case 50 ohm probes are employed on the receiver output signal.

LVDS Test 3: PCB Interconnect

This test connects Driver 4 to Receiver 2 via PCB traces. SMB connector J4 is provided to connect a signal generator to the input of Driver 4. Test point 15 is provided to monitor the input signal. Test points 14+ and 13- are located on the output of Driver 4. Test points 6+ and 7- are located on the inputs of Receiver 2. SMB connector J8 and test point 5 are located on the output of Receiver 2. A PCB option for a series 450 ohm resistor (R8) is also provided in case 50 ohm probes are employed on the receiver output signal.

LVDS Test 4: Line Driver

This test provides access to the differential outputs of Driver 3. SMB connector J3 is provided to connect to a signal generator to the input of Driver 3. Test point 9 is provided to monitor the input signal. The input of Driver 3 is terminated with a 50 ohm resistor. The output of the Driver 3 has a 100 ohm differential termination with no additional loading. The output of the Driver 3 goes to test points 10+ and 11-.

LVDS Test 5: Receiver

This test provides access to the differential inputs to Receiver 1 via SMB connectors J5 and J6. Test points 2+ and 1- are provided to monitor the input signal. Both inputs are terminated with 50 ohm resistors. SMB connector J7 and test point 3 are located on the output of Receiver 1. A PCB option for a series 450 ohm resistor (R4) is also provided in case 50 ohm probes are employed on the receiver output signal.

Jumpers on header JP26 may be removed to allow insertion of a current meter or to power the Driver and Receiver from different power supplies. (This option does not work on the present board).

The Aeroflex UTMC LVDS Evaluation board is supplied with an 18 inch twisted pair ribbon cable. Nominal impedance for this cable is 100 ohm. All wires in the cable that are not tied to signals are tied to ground.

Single ended and differential wave forms are shown in Figure 2.

Probing Hints

A Tektronix TDS 684C Digital Real Time Scope (>1Ghz bandwidth) and Tektronix P6247 Differential probes are recommended for accurate waveforms. A Tektronix P6243 single ended probe can also be used. These are only recommendations and any equivalent equipment could be used. Probe points are located on the board that allows the use of minimum lead lengths using these probes.
Differential Waveform

Single-Ended Waveforms

A ~ 1.4V
B ~ 1.0V
Ground

A - B + 0V
+V_{OD}
-V_{OD}

Figure 2. Waveforms