UT699 LEON 3FT from Aeroflex Colorado Springs

- Designed for operation in harsh environments
- Fault Tolerant architecture
- Guaranteed radiation performance
- Real-time operating system support

LEON 3FT V8 SPARC™
Microprocessor
Definitions

LEON µprocessor

LEON is a 32-bit CPU microprocessor core, based on the SPARC™ V8 RISC architecture and instruction set. The core is highly configurable, and suitable particularly for system-on-chip (SoC) designs. LEON 3FT is a Fault-Tolerant (FT) version, designed for operation in harsh, radiation-prone environments, and includes functionality to detect and correct single bit upset errors in all on-chip RAM memories.

Definitions

SPARC™ architecture

SPARC (Scalable Processor Architecture) is a RISC (Reduced Instruction Set Computing) architecture developed by Sun Microsystems. SPARC is a registered trademark of SPARC International, Inc., an organization established to create a larger ecosystem for the design by promoting, licensing, and providing conformance testing. As a result, the SPARC architecture is fully open and non-proprietary.

We offer development tools and real-time operating system support...

An advantage to working with Aeroflex’s UT699 is the extensive library of development tools. Since the UT699 is SPARC™ V8 compliant, compilers and kernels for SPARC V8 are based on industry standard development tools.

Aeroflex offers a full software development suite including a C/C++ cross-compiler system based on GCC and the Newlib embedded C-library. The BCC compiler system allows cross-compilation of C and C++ applications for the LEON 3FT family.

For multi-threaded applications, SPARC-compliant ports are available for the following operating systems: eCos, RTEMS, Linux, VxWorks, Nucleus, ThreadX and LynxOS.

To support the software development process, a simulator and a debugger are available. TSIM is a high-performance SPARC-architecture instruction simulator capable of emulating the UT699 LEON 3FT. GROMON is a debug monitor for the UT699 processor. It communicates with the UT699 debug support unit (DSU) and allows non-intrusive debugging of the complete target system.

...plus proven IP

The Aeroflex Gaisler GRLIB IP Library is an integrated set of reusable IP cores, designed for system-on-chip (SoC) development. The IP cores are centered around the common on-chip bus and use a coherent method for simulation and synthesis. The library is vendor independent, with support for different CAD tools and target technologies. A unique plug-and-play method is used to configure and connect the IP cores without the need to modify any global resources.
Aeroflex offers the best software support.

UT699 Software Development Tools (Debug)

**GRMON**
- **CODE MANAGEMENT**
  - Trace buffer, breakpoint, watch point, memory, peripheral registers
  - GNU debugger (GDB) support
  - Built-in disassembler
  - Error injection
- **INTERFACES**
  - In-system flash programming interface
  - Flexible debug interfaces: UART, JTAG, cPCI, SpaceWire

**PLATFORM**
- Eclipse IDE support
- OS: Linux/Windows

**GENERAL**
- Custom module support
- Supports future LEON roadmap

**I/O**
- Supports UT699: GPIO, timers, SpW (IEMP, common), CAN, UART, cPCI
- Loadable user-defined I/O device

**DEBugging**
- Instruction/stack trace buffer
- Non-intrusive execution time profiling
- Check-pointing capability
- Code coverage monitoring
- GNU debugger (GDB) support

**OPERATIONS**
- 64-bit time simulation
- EDAC and MMLU emulation
- Simulation performance >45 MIPS

**SYSTEM HARDWARE**
- RASTA
- ALEXIS
- Custom

**HARDWARE**
- GR-CPCI-UT699
  - 6U cPCI
  - SRAM/SDRAM
  - Flash PROM
  - Line transceivers

**Target hardware/UT699 evaluation board**
- UART or JTAG connection
- PC running GRMON on Windows or Linux

UT699 Operating Systems Options (RTOS)

<table>
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<tr>
<th>REAL-TIME OPERATING SYSTEMS</th>
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<th>PLATFORM</th>
<th>FOOTPRINT</th>
<th>COST</th>
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<tr>
<td></td>
<td>SpW</td>
<td>UART</td>
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<tr>
<td>Snapgear Linux</td>
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LEON IDE featuring

- Eclipse-based C/C++ integrated development environment
- Code entry, build system, and debugging provided
- Support for debugging on real hardware through GRMON or on a simulator through TSIM
- Support for different toolchains, templates for RTEMS/RCC, BCC, Nucleus, ThreadX, and eCos
- Source-level debugging and disassembly view
- Variables, memory, and register view
- Support for Linux and Windows host platforms

LEON Integrated Development Environment (IDE)

- Code entry
- Build System
- Debugger
- Toolchain support
- BCC
- RTEMS/RCC
- eCos
- Nucleus
- ThreadX
- Mkprom2
- PROM image

BCC = Bare-C Cross Compiler
RCC = RTEMS Cross Compiler
GDB = GNU debugger
Mkprom2 = Make prom utility
UT699 FEATURES

- Implemented on a 0.25µm CMOS technology
- Flexible static design allows up to 66MHz clock rate
- 89DMIPS throughput via 66MHz base clock frequency
- On-board programmable timers, interrupt controllers
- High-performance dual-precision IEEE-754 FPU
- Power-saving 2.5V core power supply; 3.3V I/O
- Hardened-by-design flip-flops and memory cells

UT699 CORES

AMBA bus interconnects a peripheral rich environment:

- 10/100 Base-T Ethernet port
- Integrated PCI 2.2 compatible core
- Four integrated multi-protocol SpaceWire nodes with two supporting the RMAP target protocol in hardware
- Two CAN 2.0 compliant bus interfaces
- Multifunctional memory controller with EDAC

UT699 GUARANTEED RADIATION PERFORMANCE / OPERATIONAL ENVIRONMENT

<table>
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<tr>
<th>PARAMETER</th>
<th>LIMIT</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Total Ionizing Dose (TID)</td>
<td>3E5</td>
<td>rads(Si)</td>
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<tr>
<td>Single Event Latchup (SEL)</td>
<td>&gt;108</td>
<td>MeV-cm²/mg</td>
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<tr>
<td>Neutron Fluence</td>
<td>1.0E14</td>
<td>n/cm²</td>
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UT699 BLOCK DIAGRAM

UT699 LEON 3FT

- IEEE754 FPU
- MUL/DIV
- MMU

AHB interface

2X4K D-cache
2X4K I-cache

Debug support unit

4x SpaceWire

Serial/JTAG debug link

PCI bridge

Ethernet MAC

AHB AHB

AHB/APB bridge

Memory controller

AHB arbiter

8/32-bit memory bus

512MB non-volatile
512MB I/O
Up to 1GB SRAM
Up to 1GB SDRAM

LIART
Timers
IqqCtrl
I/O port

NOTIONAL SINGLE BOARD COMPUTER

UT699 LEON 3FT

RS-422

8MB EDAC SRAM

4MB EDAC non-volatile memory

Dedicated SpW Links

Ethernet PHY

Port 1
Port 2
Port 3
Port 4
LEON UT699 3FT SPARC™ V8
MICROPROCESSOR EVALUATION BOARD

The GR-CPCI-UT699 development board is capable of running at a system clock speed of 66MHz. The board is a 6U cPCI form factor and can also be used in a standalone bench-top configuration. The board supports 32-bit/33MHz PCI, 10/100 Base-T Ethernet, four SpaceWire ports capable of running up to 200Mbits/s, two CAN ports, on-board FLASH, SRAM, and SDRAM. A socket for a PROM device and a USB debug port are also on-board.

ALExIS

ALExIS (Aeroflex LEON Experimenter’s Interface System) is a ready-to-run development platform for customer applications with flexible architecture supporting quick path-to-flight after development. Flight and non-flight versions of the UT699-based single board computer of the ALExIS are available. The ALExIS platform provides two cPCI slots for future card expansion, and pre-loaded operating systems and applications drivers.

RASTA

The Aeroflex Gaisler implementation of the RASTA (Reference Avionics System Testbed Activity) aims to provide a standardized hardware and software infrastructure for development, prototyping and validation of on-board systems. It allows quick and easy integration of complete systems in a lab environment, using standardized interfaces and connectors. It also provides access to LEON3 technology (through FPGA, ASIC, or products like UT699).