FEATURES

- Up to 50,000,000 2-input NAND equivalent gates with a 1.0V Core using standard cell architecture
- Toggle rates up to 5.0 GHz
- Advanced 90nm silicon gate CMOS processed in a commercial fab
- Operating voltages: 2.5V and 1.8V I/O; 1.0V core
- Radiation hardened from 100 krads(Si) to 1 Mrads(Si) total dose available
- Comprehensive set of core standard cells with multiple $V_t$ options for optimizing speed and power
- Design support for Mentor Graphics®, Synopsys®, Verilog and VHDL design languages on Sun™ and Linux workstations
- Power dissipation of $7 \text{nW/MHz/gate}$ at $V_{DDCORE}$ 1.0V and 20% duty cycle
- External chip capacitor attachment option available to space quality levels (for improved SSO response)
- UT90nHBD ASIC technology is available under Aeroflex’s Accreditation of Trust Category 1A from design through device qualification and delivery.
- QML Class Y non-hermetic Flip Chip ceramic packaging
- Standard Microelectronics Drawing - 5962-14B01

PRODUCT DESCRIPTION

Cobham Semiconductor Solutions’ (formerly Aeroflex) high-performance UT90nHBD Hardened-by-Design ASIC standard cell family features densities up to, and beyond 50,000,000 equivalent NAND2 gates.

The deep submicron ASIC family uses a highly efficient standard cell architecture for the internal cell instantiation. Combined with state-of-the-art place and route tools, the area utilization and internal cell interconnect is maximized using eight levels of copper metal interconnect.

Extensive Cell Library

The UT90nHBD standard cell family is supported by an extensive cell library with over 900 elements. User selectable options for cell configurations include scan for all register elements, output drive strengths (1x to 30x) and transistor threshold voltages ($LVT, RV_t$).

Refer to Cobham’s UT90nHBD Design Manual for complete cell listing and details.

SerDes Intellectual Property (IP)

The UT90nHBD SerDes is RadHard, quad channel, Serializer/Deserializer (SerDes) IP targeted for 10G XAUI applications in 90nm CMOS SoC ASIC designs. This SerDes macro block is a half-rate architecture providing a robust transmitter with 8/10/16/20:1 serialization, Feed Forward Equalization (FFE) and pre-emphasis, and a robust receiver with 1:8/10/16/20 deserialization. Included is a low jitter reference PLL which uses an external clock input to provide a common clock across 4 Tx/Rx lanes. With 8b/10b encoding, this UT90nHBD SerDes can also be used as a general purpose serializer/deserializer. Single and dual channel SerDes macro block are also available.

Cobham Gaisler IP

We offer Cobham Gaisler LEON3 and RTL based IP which can be viewed at www.cobham.com/gaisler.
I/O Buffers
The UT90nHBD library offers extensive I/O cell options. The I/O library contains 36 different general purpose CMOS functional I/O pads. A rich set of LVDS inputs and outputs support data rates up to 1.2Gbps with optional on-chip terminations. The LVDS family of buffers include several drive strengths for point-to-point, multi-point, and Bus-LVDS applications. The LVDS buffers have programmable slew rate control. 2.5V and 1.8V LVDS cells are available to optimize for speed and power in the system design.

Other I/O buffer features and options include:

- Basic Input, Output, and Bi-directional
- 9mA and 18mA drive strength
- Slew rate control
- Schmitt Trigger
- Tri-State
- Open Drain
- SSTL 1.8V/2.5V

Cold Sparring
The UT90nHBDI/O library includes a set of cold sparing I/O cells that enables the user to design for system redundancy. These cold sparing cells present a high input impedance to the system interface when powered off assuring that the cold spared redundant device does not draw power.

Macro Cells
The UT90nHBD library includes a macro cell library that enables system-on-a-chip (SOC) design. The following macros are currently available:

- Clock Generator PLL
- 3.125 Gbps per-lane SerDes Macro, in 1, 2, and 4-lane configuration for data rate of up to 10 Gbps
- Embedded die temperature resistor

Embedded SRAM
Cobham offers a comprehensive set of compiled embedded memories to meet your ASIC architectural needs. Features include:

- Single and Dual Port SRAM compiler
- Single and Two Port Register File compiler
- Operating frequencies of 400MHz and higher
- Optional EDAC RTL generation: 1 or 2 bit detect, 1 bit correct
- Configurable word write mask
- Optional integrated BIST Mux/Collar
- All standard EDA views supported

Clock Driver Distribution
Cobham design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices. The UT90nHBD PLL’s all include optional external clock feedback to support clock de-skew applications.

Speed and Performance
Cobham specializes in high-performance circuits designed to operate in harsh military and radiation environments. The UT90nHBD library offers cells in both regular Vt and low Vt allowing the user to trade speed for power. The cells can be mixed on the same die providing local solutions for critical paths without sacrificing full chip power consumption.

Power Dissipation and Power Estimation Tools
Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. Radiation-tolerant processes exhibit power dissipation that is typical of CMOS processes. A power estimation spreadsheet that is useful for architecture trade-off analysis is available in the customer toolkit. For a more rigorous power estimating methodology, the synthesis library in the customer design toolkit supports pre-layout and post-layout power analysis. For additional information, refer to the Cobham UT90nHBD Design Manual or consult with a Cobham Applications Engineer.

Packaging
Both Flip Chip and Wire Bond packaging is available for the UT90nHBD ASICs. Standard pin counts range from 624 to 1752 in both ceramic CGAand Column attach options. Heat sink and decoupling capacitors are available in the Class Y package.

UT90nHBD SerDes Intellectual Property (IP)

- Available in UT90nHBD ASIC library based upon an advanced 90nm silicon gate CMOS process in a commercial fab
- TID hardness > 1MRad (Si)
- SEU/Soft Error immune; no high-speed link downtime
- 3.125Gbps maximum data rate per lane
- 10Gbps data throughput when 8b/10b encoding is used with this four lane macro
- PLL reference: 156.25MHz or 312.5MHz
- Low 240mW per lane power consumption
The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.
### Data Sheet Revision History

<table>
<thead>
<tr>
<th>REV</th>
<th>Revision Date</th>
<th>Description of Change</th>
<th>Page(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>8-22-16</td>
<td>Added Cobham data sheet template.</td>
<td>All</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added SerDes information.</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edited Macro Cell bullets.</td>
<td>2</td>
</tr>
</tbody>
</table>