

The most important thing we build is trust

FEATURES

- ❑ LVDS dual transceiver or quad repeater
 - One part, dual function:
 - Full-duplex dual transceiver
 - Half-duplex quad repeater
- ❑ Data Rates up to 1.25 Gbps per channel
- ❑ Protocol Independent
- ❑ Cold sparing all pins
- ❑ Low Propagation Delay
- ❑ Low Channel-to-Channel Skew
- ❑ Supports up to 1 meter of FR4 PCB or 10 meters of cable up to 1.25Gbps
- ❑ Single 2.5V +/-5% power supply
- ❑ Selectable 3.5mA or 7.0mA output drive currents
- ❑ Low power standby mode
- ❑ Enable/Enable* input to disable LVDS drivers
- ❑ Fail-safe function for loss of signal detection
- ❑ Compatible with TIA/EIA-644A LVDS standard
- ❑ QML-Q and QML-V Qualification Pending
- ❑ Package Information:
 - 71-Pin Ceramic Land Grid Array (C-LGA)
 - Small QML package Size: 9.0 mm x 10 mm, 1 mm Pad Pitch

OPERATIONAL ENVIRONMENT

- ❑ Temperature Range: $-55^{\circ}\text{C} \leq T_c \leq +105^{\circ}\text{C}$
- ❑ Total Dose: 100 kRad (Si)
- ❑ SEL Immune: $\leq 100 \text{ MeV-cm}^2/\text{mg}$

APPLICATIONS

- ❑ High Speed Dual LVDS Transceiver
- ❑ High-Speed Quad LVDS Repeater
- ❑ Mission Critical FPGA LVDS I/O Protection

INTRODUCTION

The UT54LVDS454 is a single high performance device that can be configured by pin connection through PCB high-speed signal layout for either of two functions: 1) Dual LVDS transceiver, or 2) Quad LVDS repeater. Both configurations are intended for high-speed, high-reliability, space, and other harsh environment serial link applications. See block diagrams as Figures 1.2 and 1.3, below.

The all-pins cold-sparing feature, coupled with the user-supplied external RX/TX differential 100Ω terminations, and small LGA package footprint, provides for maximum application flexibility in systems with mission critical serial link full redundancy requirements.

In addition, the user-selectable TX drive current and back-termination options, enables maximum system flexibility for user optimization of device power dissipation.

For short links ($\leq 10\text{cm}$), the TX drive current can be reduced by half to 3.5mA and the back-termination resistor not installed while still providing acceptable signal integrity (SI) and BER performance at reduced power consumption. For longer links ($> 10\text{cm}$), the TX drive current is set to 7.0mA in conjunction with the back-termination resistor installed for improved SI and BER performance at still low power consumption.

1.0 FUNCTIONAL DESCRIPTION

Overview

Figure 1.1 illustrates the functionality of a single channel of the LVDS Transceiver and Figure 1.2 shows the device block diagram. The device is comprised of four independent LVDS channels, all of which are controlled by a common digital section.

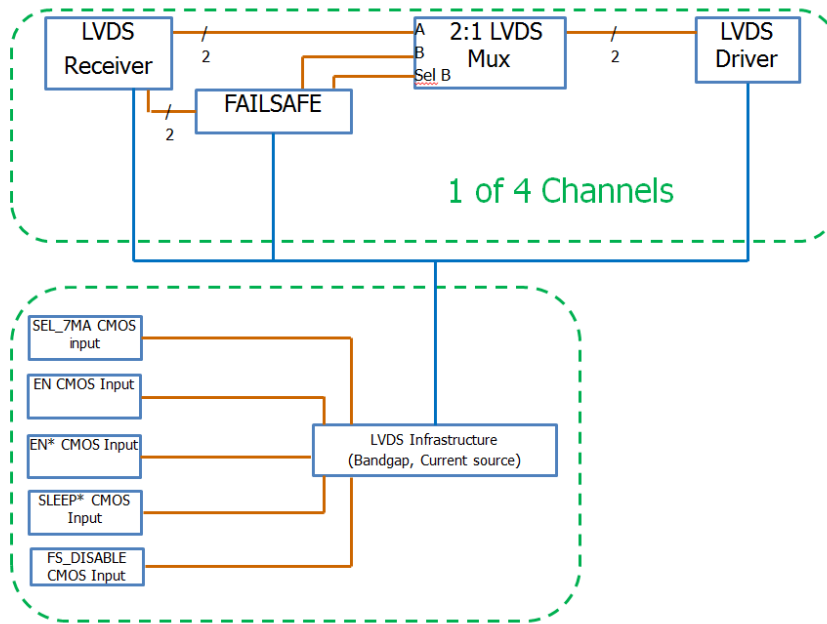


Figure 1.1: UT54LVDS454 Dual Transceiver / Quad Repeater Single Channel Functional Block Diagram

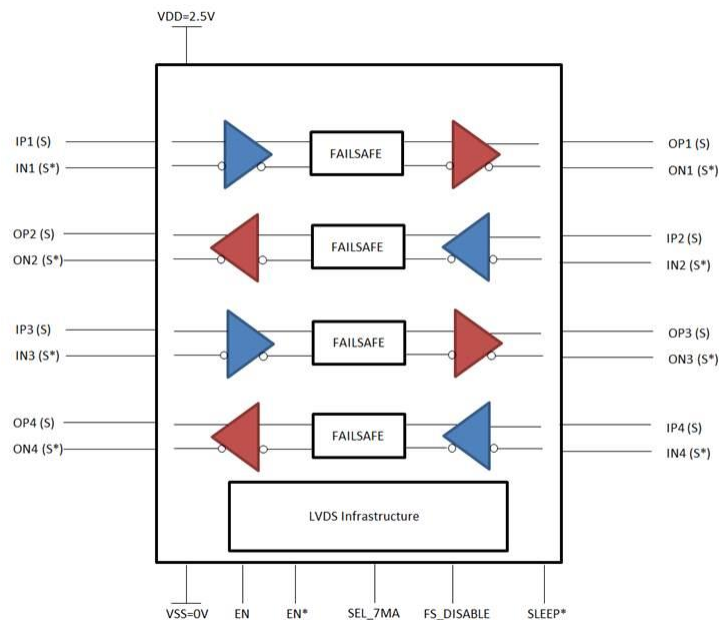


Figure 1.2: UT54LVDS454 Dual Transceiver Configuration Block Diagram

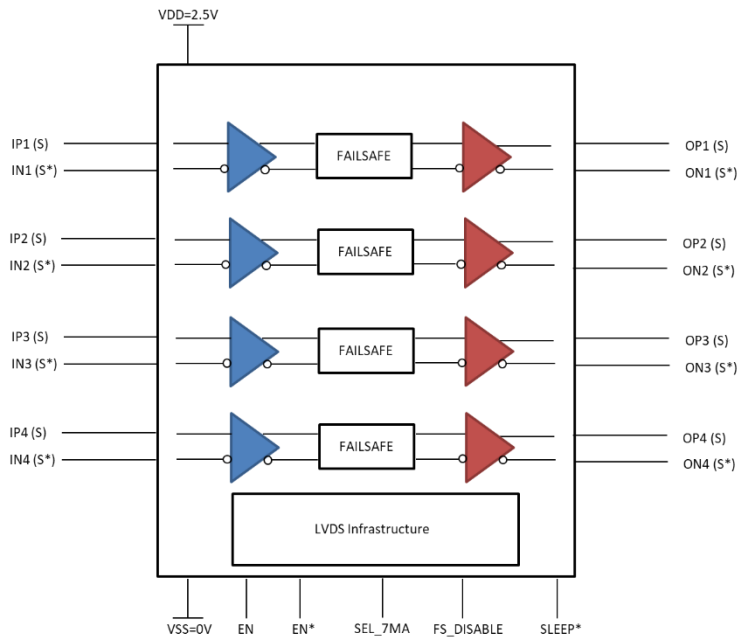


Figure 1.3: UT54LVDS454 Quad Repeater Configuration Block Diagram

UT54LVDS454 Input Receiver

The UT54LVDS454 Receiver (RX) input buffers operate using the Low Voltage Differential Signaling (LVDS) I/O standard. The inputs must be externally terminated with 100Ω between the differential signals. The input buffers support an amplitude range of 100mVp-p to $2,500\text{mVp-p}$ differential voltage. The common-mode input range is 0.1V to $\text{VDD}-0.1\text{V}$, with a 150mV differential input around the common-mode input voltage. An input fail safe circuit detect function is implemented and activated with `FS_DISABLE` pin set to logic low. With the fail-safe function enabled, if an input signal edge rate falls below 1MHz rate, the respective LVDS output is driven to a logic 1 state.

UT54LVDS454 Output Driver

The UT54LVDS454 Output Driver (TX) operates using the Low Voltage Differential Signaling (LVDS) I/O standard. Each output must be terminated at the far-end RX in 100Ω for the 3.5mA drive option, or both at the near-end TX and the far-end RX for the 7mA drive option. The TX output differential amplitude range is 280 to 400mVp-p for either (a) 3.5mA , 100Ω load, or (b) 7.0mA , 50Ω load. The output common mode voltage range is $1.25\text{V} \pm 10\%$.

2.0 DEVICE PIN DESCRIPTION

Input-Output and Control Pin Description

Table 2.1: UT54LVDS454 Input-Output and Control Pin Description

Pin Name	Description
IP#	Positive LVDS input. # associated with the channel corresponding to the input pin.
IN#	Negative LVDS input. # associated with the channel corresponding to the input pin.
OP#	Positive LVDS output. # associated with the channel corresponding to the output pin.
ON#	Negative LVDS output. # associated with the channel corresponding to the output pin.
SLEEP*	Active Low, Ultra-Low Power Sleep pin – LVCMOS Input.
EN	Active High Transmitter Enable – LVCMOS Input.
EN*	Active Low Transmitter Enable – LVCMOS Input.
SEL_7MA	Active High 7mA drive current select pin. 3.5mA when low – . LVCMOS Input.
FS_DISABLE	Active High failsafe disable – . LVCMOS Input.
VSS	Power Supply Ground Return. 0V.
VDD	Positive Power Supply, 2.5V nominal.

Table 2.2: UT54LVDS454 Package Pad Location and Function

PACKAGE PAD LOCATION	PACKAGE PAD NAME	PACKAGE PAD FUNCTION AND TYPE
A01	<no pad>	Land #1 - No Connect (N/C)
LVDS Transmit (TX) Differential Signal Pairs		
G08	OP1	Positive LVDS channel 1, output
H08	ON1	Negative LVDS channel 1, output
J02	OP2	Positive LVDS channel 2, output
J03	ON2	Negative LVDS channel 2, output
A03	OP3	Positive LVDS channel 3, output
A02	ON3	Negative LVDS channel 3, output
B08	OP4	Positive LVDS channel 4, output
C08	ON4	Negative LVDS channel 4, output
LVDS Receive (RX) Differential Signal Pairs		
J06	IP1	Positive LVDS channel 1, input
J07	IN1	Negative LVDS channel 1, input
G01	IP2	Positive LVDS channel 2, input
H01	IN2	Negative LVDS channel 2, input
B01	IP3	Positive LVDS channel 3, input
C01	IN3	Negative LVDS channel 3, input
A06	IP4	Positive LVDS channel 4, input
A07	IN4	Negative LVDS channel 4, input
Control Signals		
C06	FS_DISABLE	Failsafe disable, input
D02	SLEEP*	Sleep function, input
E02	SEL_7MA	TX Output Drive select, input
F02	EN*	TX Output Enable, input
H04	EN	TX Output Enable, input
Cobham-Only Signals		
B05	COBHAM USE ONLY	Connect R _{EXT} =20KΩ to VSS
Power		
B06	VDD	POWER
C04	VDD	POWER
C07	VDD	POWER
D03	VDD	POWER
D04	VDD	POWER
D05	VDD	POWER
E01	VDD	POWER
E03	VDD	POWER
E05	VDD	POWER
E06	VDD	POWER
E08	VDD	POWER
F03	VDD	POWER
F04	VDD	POWER
F06	VDD	POWER
G02	VDD	POWER

G03	VDD	POWER
G05	VDD	POWER
G06	VDD	POWER
G07	VDD	POWER
H03	VDD	POWER
H06	VDD	POWER
Ground		
A04	VSS	GROUND
A05	VSS	GROUND
A08	VSS	GROUND
B02	VSS	GROUND
B03	VSS	GROUND
B04	VSS	GROUND
B07	VSS	GROUND
C02	VSS	GROUND
C03	VSS	GROUND
C05	VSS	GROUND
D01	VSS	GROUND
D06	VSS	GROUND
D07	VSS	GROUND
D08	VSS	GROUND
E04	VSS	GROUND
E07	VSS	GROUND
F01	VSS	GROUND
F05	VSS	GROUND
F07	VSS	GROUND
F08	VSS	GROUND
G04	VSS	GROUND
H02	VSS	GROUND
H05	VSS	GROUND
H07	VSS	GROUND
J01	VSS	GROUND
J04	VSS	GROUND
J05	VSS	GROUND
J08	VSS	GROUND

2.2 PINLIST – PACKAGE CONFIGURATION: TOP VIEW

Table 2.3. Pin List / Package Configuration – TOP VIEW

	8	7	6	5	4	3	2	1	
J	VSS	IN1	IP1	VSS	VSS	ON2	OP2	VSS	J
H	ON1	VSS	VDD	VSS	EN	VDD	VSS	IN2	H
G	OP1	VDD	VDD	VDD	VSS	VDD	VDD	IP2	G
F	VSS	VSS	VDD	VSS	VDD	VDD	EN*	VSS	F
E	VDD	VSS	VDD	VDD	VSS	VDD	SEL_7 MA	VDD	E
D	VSS	VSS	VSS	VDD	VDD	VDD	SLEEP*	VSS	D
C	ON4	VDD	FS_DIS ABLE	VSS	VDD	VSS	VSS	IN3	C
B	OP4	VSS	VDD	20KΩ TO VSS	VSS	VSS	VSS	IP3	B
A	VSS	IN4	IP4	VSS	VSS	OP3	ON3	N/C	A
	8	7	6	5	4	3	2	1	

3.0 ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Table 3.1: Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
VDD	LVDS Power Supply	-0.3	3.6	V
VSS	LVDS Ground	-0.3	+0.3	V
V _{IN, LVCMOS}	LVCMOS Input / Output Signals	-0.3	VDD	V
ESD _{LVDS}	LVDS ESD Rating (HBM)	4k	-	V
ESD _{NON-LVDS}	Non-LVDS ESD Rating (HBM)	2k	-	V
θ _{JC}	Thermal Resistance (junction to case)		12.7	°C/W
T _J	Junction Temperature		132	°C
T _{STG}	Storage Temperature	-65	125	°C
P _D ^(2,3)	Maximum package power dissipation		500	mW

NOTES:

- Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
- Test per MIL-STD-883, Method 1012.
- Per MIL-STD-883, method 1012.1, section 3.4.1, $P_D = (T_J(\text{max}) - T_C(\text{max})) / \theta_{JC}$

4.0 OPERATIONAL ENVIRONMENT

Table 4.1: Operational Environment

SYMBOL	PARAMETER	LIMIT	UNITS
TID ⁽¹⁾	Total Ionizing Dose	1.0E5	rad(Si)
SEL ⁽¹⁾	Single Event Latch-up Immunity	≤100	MeV-cm ² /mg

NOTES:

- TID, SEL Guaranteed by design. Test Pending

5.0 RECOMMENDED OPERATING CONDITIONS

Table 5.1: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VDD	LVDS Power Supply (2.5V ± 5%)	2.375	2.5	2.625	V
VSS	Ground		0		V
V _{IN, LVDS}	Input Voltage on any LVDS input pin	0.0		VDD	V
V _{IN, LVCMOS}	Input Voltage on any LVCMOS input pin	0.0		VDD	V
T _C	Case Temperature Range	-55		105	°C
T _J	Junction Temperature			125	°C

NOTES:

6.0 ELECTRICAL CHARACTERISTICS

6.1 DC ELECTRICAL CHARACTERISTICS

VDD=2.5V+/-5%, -55°C < T_c < +105°C, unless otherwise noted.

Table 6.1.1: LVDS I/O DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCMR	Input Common Mode Voltage Range	VID = 150mV	0.1	1.25	VDD-0.1	V
VID_HYS	Differential Input Voltage Hysteresis	VCM = 1.25V		25		mV
ICS	Cold Spare Input Current IP/N	VIN = VDDMAX, VDD = VSS = 0V	-		75	μA
OCS	Cold Spare Output Current OP/N	VOUT = VDDMAX, VDD = VSS = 0V	-		5	μA
IIN_L	Input Current Low	IP, IN [1:4] = VSS	-50			μA
IIN_H	Input Current High	IP, IN [1:4] = VDD			50	μA
VOS ^(1,2)	Output Common-Mode Offset Voltage	LVDS Outputs		1.33		V
ΔVOS ^(1,2)	Change in VOS Between Complementary Logic States		-25		+25	mV
AIDD ⁽²⁾	VDD Active Supply Current	K28.5 pattern @1.25Gbps			102	mA
QIDD ⁽²⁾	VDD Quiescent Supply Current	EN/EN* Inactive (OP/ON Disabled)			75	mA
IDDSL ⁽²⁾	VDD Supply Sleep Current	SLEEP* Active			70	μA
IOS_sink ⁽²⁾	Output Short Circuit Current	OP/ON = VDD, VDD = VDDMAX	4.0		8.0	mA
IOS_source ⁽²⁾	Output Short Circuit Current	OP/ON = VSS, VDD = VDDMAX	-10.5	-8.2	-5.9	mA
V _{ID}	Input Amplitude, diff	Differential, Peak-to-Peak VCM = 1.25V	0.1		VDD	V
V _{OD} ^(1, 2)	Output Amplitude, diff.	Differential, Peak-to-Peak	250	330	400	mV
ΔV _{OD} ⁽²⁾	Change in V _{OD,LVDS} between complementary logic states	LVDS Outputs	-20		20	mV
P _{total} ⁽²⁾	Power Dissipation	1.25Gbps, all channels operating		170	274	mW
CIN_P ⁽³⁾	Input Capacitance IP#	IP/IN to VSS		5.0		pF
CIN_N ⁽³⁾	Input Capacitance IN#			5.0		pF
COUT_P ⁽³⁾	Output Capacitance OP#	OP/ON to VSS		6.0		pF
COUT_N ⁽³⁾	Output Capacitance ON#			6.0		pF

NOTES:

1. TX drive current of 3.5mA selected, 100Ω load
2. TX drive current of 7mA selected, 50Ω load
3. Reference values only. Not guaranteed or tested.

Table 6.1.2: LVCMOS I/O DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIH	CMOS high level input voltage		VDD*0.7		-	V
VIL	CMOS low level input voltage		-		VDD*0.3	V
IIH	CMOS high level input current	VIN=VDD	-		20	μA
IIL	CMOS low level input current	VIN=VSS	-10		-	μA
ICS	Cold-Spare Input Current	VIN = VDDMAX, VDD = VSS = 0V	-		10	μA

6.2 AC ELECTRICAL CHARACTERISTICS

6.2.1 AC ELECTRICAL CHARACTERISTICS: TIMING PARAMETERS

VDD=2.5V+/-5%, -55°C < Tc < +105°C, unless otherwise noted.

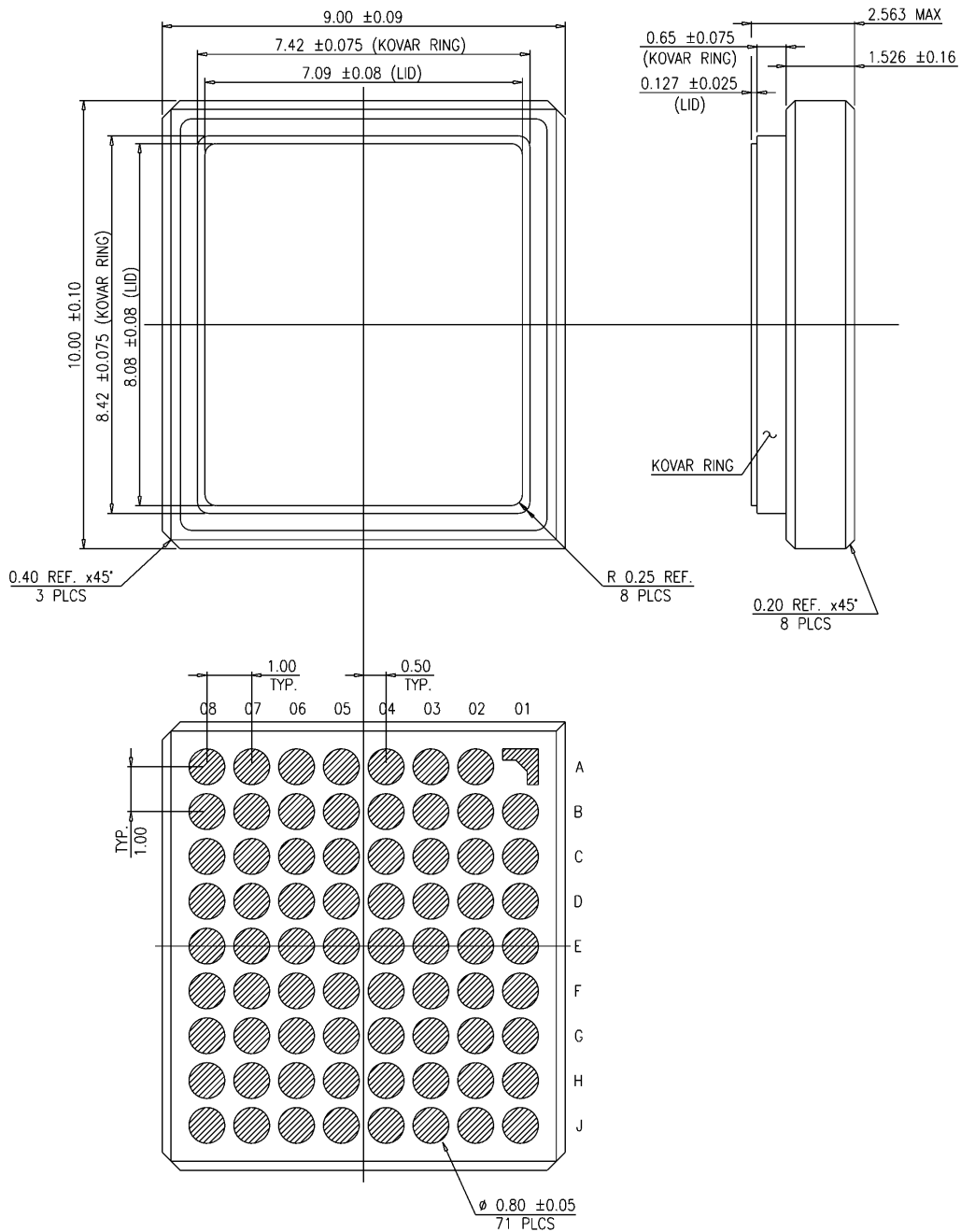
Table 6.2.1: Timing Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DR	Data Rate / Channel		0.002		1.25	Gbps
DC1 ⁽⁴⁾	LVDS Output Duty Cycle	50% duty cycle input signal, 200MHz ⁽¹⁾	50.0	50.1	50.2	%
DC2 ⁽⁴⁾	LVDS Output Duty Cycle	50% duty cycle input signal, 200MHz ⁽²⁾	49.9	50.0	50.1	%
tPHLD1 ⁽⁴⁾	LVDS High-Low Output prop. delay	100Ω load ⁽¹⁾	2.1	2.7	3.6	ns
tPLHD1 ⁽⁴⁾	LVDS Low-High Output prop. delay		2.1	2.7	3.6	ns
tPHLD2 ⁽⁴⁾	LVDS High-Low Output prop. delay	50Ω load ⁽²⁾	2.0	2.6	3.5	ns
tPLHD2 ⁽⁴⁾	LVDS Low-High Output prop. delay		2.0	2.6	3.5	ns
tHLT1 ⁽³⁾	LVDS High-Low Output transition time	100Ω load ⁽¹⁾	665	676	676	ps
tLHT1 ⁽³⁾	LVDS Low-High Output transition time		646	663	663	ps
tHLT2 ⁽³⁾	LVDS High-Low Output transition time	50Ω load ⁽²⁾	215	258	282	ps
tLHT2 ⁽³⁾	LVDS Low-High Output transition time		215	241	277	ps
TJ1 ⁽³⁾	Total Jitter	CRPAT pattern		60	127	ps p-p
TJ2 ⁽⁴⁾	Total Jitter	625MHz clock pattern			5.0	ps rms
TEN ⁽⁴⁾	Device Output Enable time	Time from EN↑ & EN*↓ to ON/OP going active	3.3	4.2	5.6	ns
TDIS ⁽⁴⁾	Device Output Disable time	Time from EN↓ & EN*↑ to ON/OP going tri-state	1.5	2.1	3.1	ns
TSLEEP ⁽⁴⁾	Device sleep time	Time from SLEEP*↓ to ON/OP going tri-state (VOS)	3.3	4.3	5.8	ns
TWAKE ⁽⁴⁾	Device wake time	Time from SLEEP*↑ to ON/OP going active	2.4	2.8	3.4	us
TFAILSAFE ⁽⁴⁾	Failsafe timeout after loss of signal	Time from VDIN<VTH, FS_DISABLE=VSS	0.3	0.6	1	us
TSKD1 ⁽⁴⁾	Differential Output Pulse Skew	Channel-N tPLHD-tPHLD			30	ps
TSKCC ⁽⁴⁾	Output Channel to Channel Skew	All Channels tPLHD-tPHLD			50	ps

NOTES:

1. TX drive current of 3.5mA selected, 100Ω load
2. TX drive current of 7mA selected, 50Ω load
3. Guaranteed by Characterization
4. Guaranteed by Design

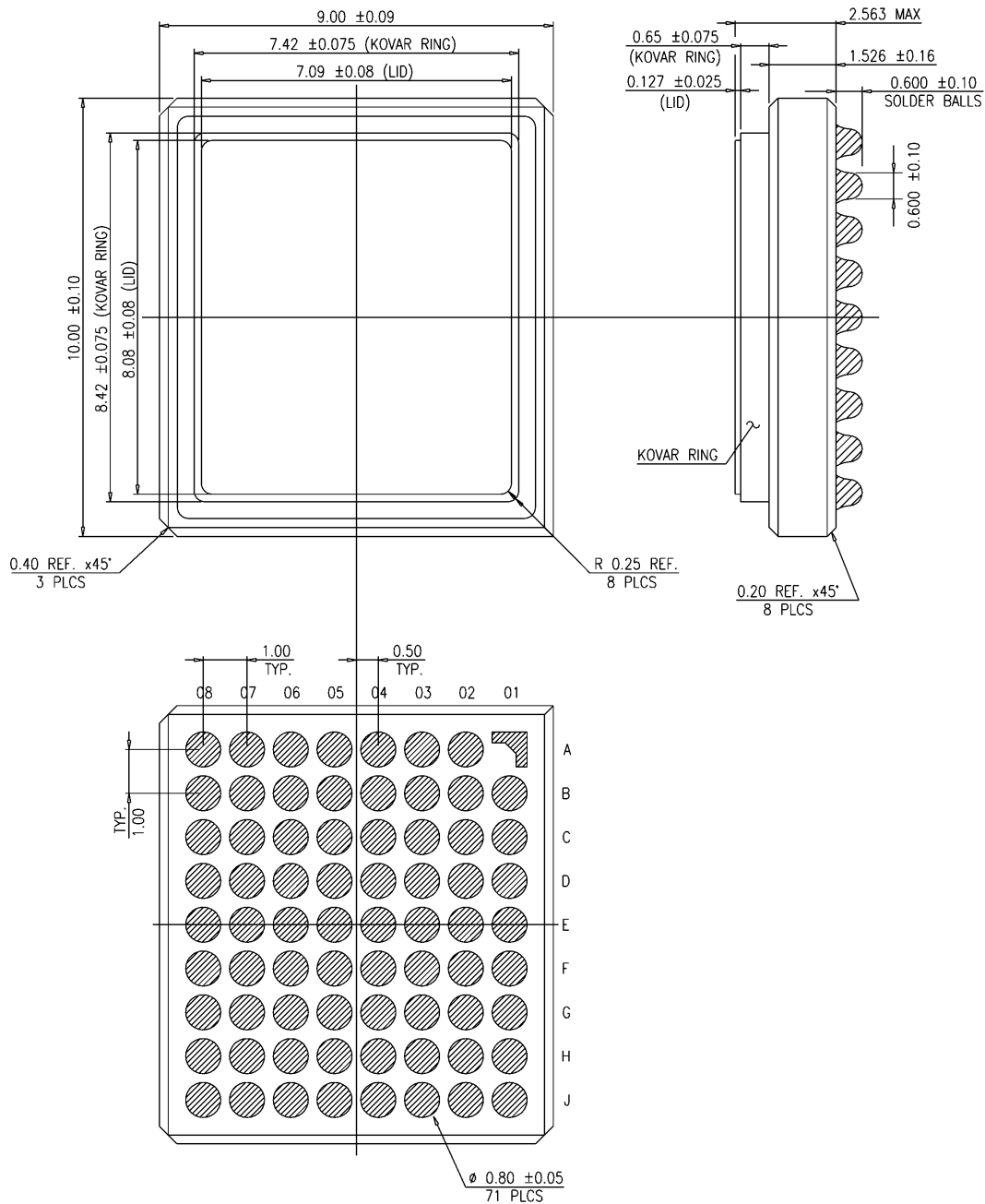
7.0 PACKAGING DRAWINGS



NOTES

1. UNITS ARE MILLIMETERS
2. LID IS CONNECTED TO VSS
3. EXPOSED-METAL PLATING PER MIL-PRF-38535
ELECTROLESS NICKEL 4.0um NOMINAL [2.54-8.89 limits]
IMMERSION GOLD 0.03-0.10um

Figure 7.1: 71-Pin Ceramic Land Grid Array (C-LGA) Package



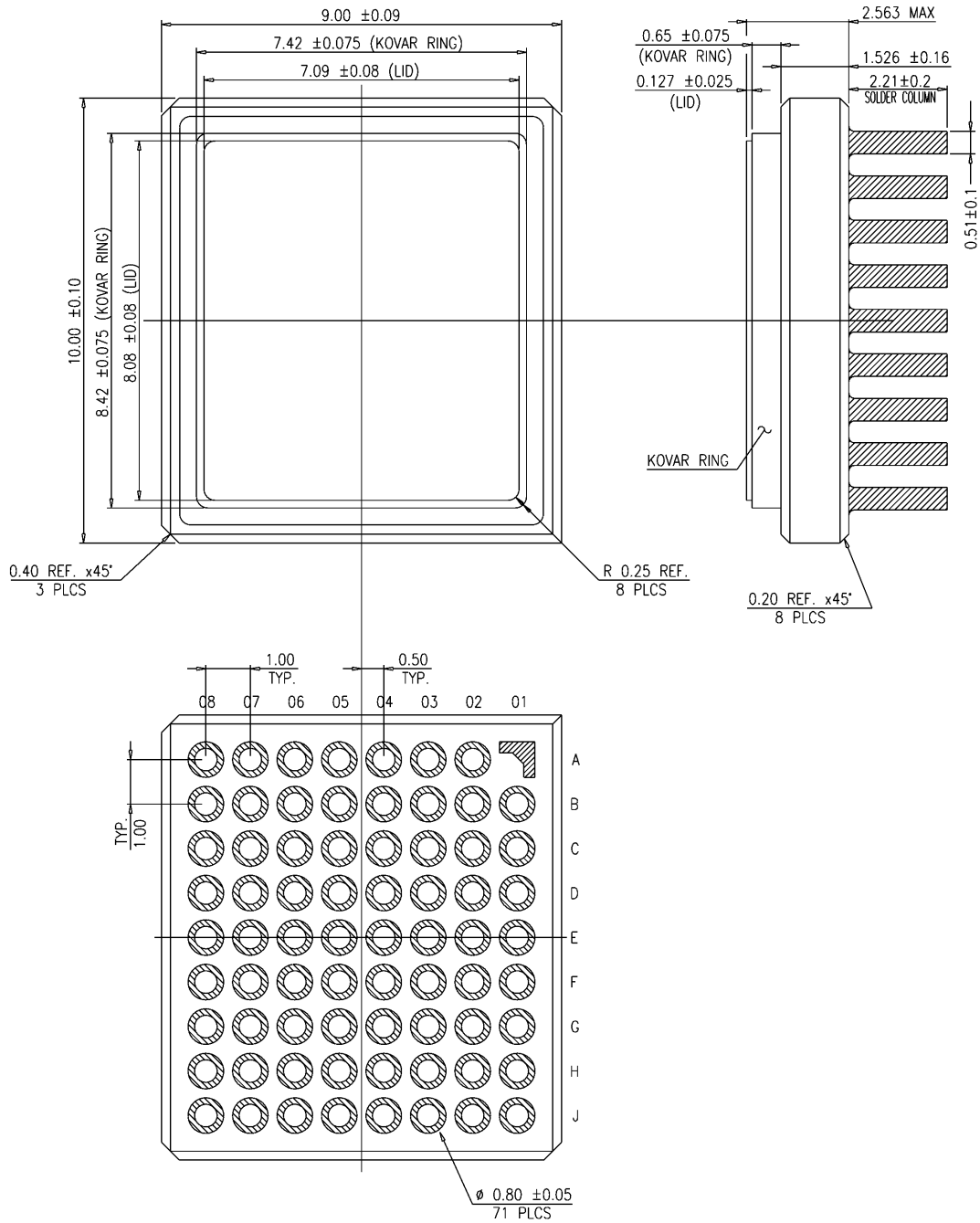
NOTES

1. UNITS ARE MILLIMETERS
2. LID IS CONNECTED TO VSS
3. EXPOSED-METAL PLATING PER MIL-PRF-38535
ELECTROLESS NICKEL 4.0µm NOMINAL [2.54-8.89 limits]
IMMERSION GOLD 0.03-0.10µm
4. SOLDER BALLS ARE 90Pb/10Sn COMPOSITION, ATTACHED WITH 37Pb/63Sn EUTECTIC.

Figure 7.2: 71-Pin Ceramic Ball Grid Array (C-BGA) Package

Notes:

- (1) Solder balls are available for prototypes and engineering samples only, as they are not QML-qualified.
- (2) The dimensions shown for the attached solder balls are approximate.



NOTES

1. UNITS ARE MILLIMETERS
2. LID IS CONNECTED TO VSS
3. EXPOSED-METAL PLATING PER MIL-PRF-38535
ELECTROLESS NICKEL 4.0um NOMINAL [2.54-8.89 limits]
IMMERSION GOLD 0.03-0.10um

Figure 7.3: 71-Pin Ceramic Column Grid Array (C-CGA) Package

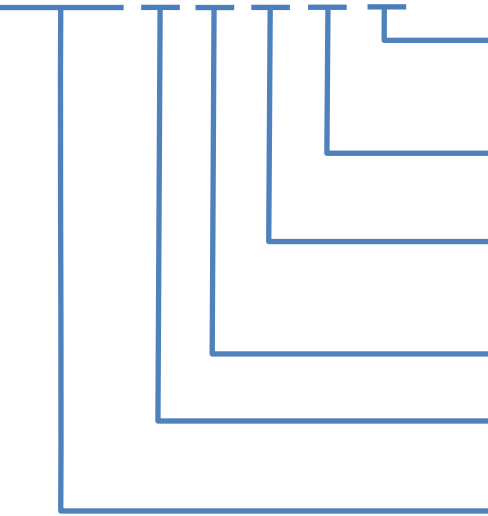
8.0 ORDERING INFORMATION

8.1 COBHAM PART NUMBER ORDERING INFORMATION

Generic Datasheet Part Numbering

UTxxxxx

*** * * *



Lead Finish: (Notes: 1)

- (A) = Hot Solder Dipped or Tinned
- (C) = Gold
- (F) = Solder Column (Copper wound, solder coated)

Screening Level: (Notes: 2, 3, 4, 5, 6, 7)

- (P) = Prototype Flow (Temperature Range: 25°C only)
- (C) = HiRel Flow (Temperature Range: -55°C to +105°C)

Case Outline: (Note: 6,7)

- (Z) = 71-Ceramic Land Grid Array
- (S) = 71-Ceramic Column Grid Array
- (C) = 71-Ceramic Ball Grid Array

Radiation Hardness Assurance:

- (-) = No Radiation Assurance

Device Type:

- (500) = Description of unique device type (Could be density, speed grade, etc).

UT54LVDS454 – High Speed LVDS Dual Transceiver

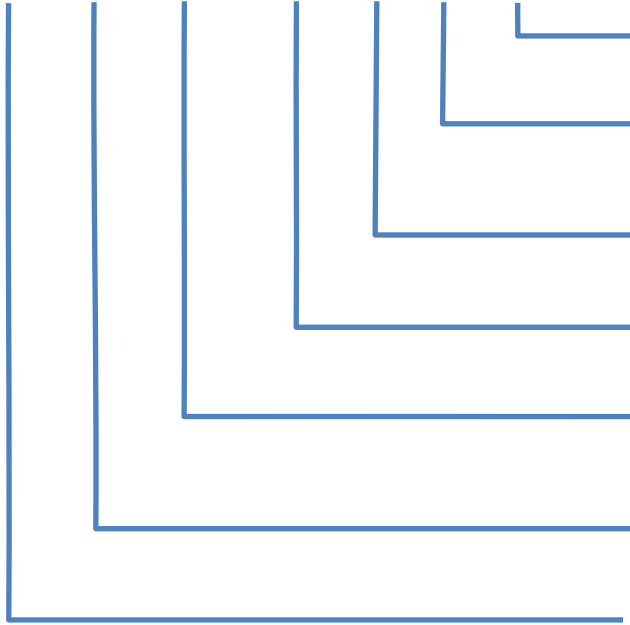
NOTES:

1. Lead finish (A, C, or F) must be specified.
2. Prototype Flow per Cobham Manufacturing Flows Document. Radiation is neither tested nor guaranteed.
3. HiRel Flow per Cobham Manufacturing Flows Document. Radiation TID tolerance may not be ordered.
4. For ceramic Land Grid Array (LGA) packages, the lead finish is "C" (Gold-only). For Ball Grid Arrays (BGA) packages, the lead finish is "A" (Hot Solder Dipped). For Column Grid Array (CGA) packages, the lead finish is "F" (Solder Column).
5. Contact factory to define alternative screening options
6. Ball Grid Array (BGA) Case Outline is only available for Prototype Flow Screening Level. (BGA Case Outline is not available for HiRel Flow Screening Level.)
7. All Case Outline options (i.e. LGA, BGA, CGA) are available for Prototype Flow Screening Level.

8.2 SMD PART NUMBER ORDERING INFORMATION

SMD Part Numbering

5962 * ***** ** * * *



Lead Finish: (Notes: 1)

(C) = Gold
(F) = Solder Column (Copper wound, solder coated)

Case Outline: (Note: 2)

(X) = 71-Ceramic Land Grid Array
(Y) = 71-Ceramic Column Grid Array

QML Class: (Note: 3)

(Q) = Class Q
(V) = Class V

Device Type:

(01) = UT54LVDS454 (Temperature Range: -55C to +105C)

SMD Project Number:

(xxxxx) = UT54LVDS454 High Speed LVDS Transceiver

Radiation Hardness Assurance: (Notes: 4)

(R) = 100 krad(Si)

Federal Stock Class Designator

NOTES:

1. Lead finish (C or F) must be specified.
2. For ceramic Land Grid Array (LGA) packages, the lead finish is "C" (Gold-only). For Column Grid Array (CGA) packages, the lead finish is "F" (Solder Column)
3. Contact factory to determine alternative screening options.
4. A radiation hardness assurance level must be selected.

10.0 REVISION HISTORY

Date	Revision	Change Description
09/06/2018	0.0.1	Advanced Datasheet – Initial revision
10/23/2018	0.0.2	Advanced Datasheet – Update 1
10/30/2018	0.0.3	Advanced Datasheet – Update 2
02/05/2019	0.0.4	Advanced Datasheet – Update 3
08/28/2019	0.0.5	Preliminary Datasheet – Update 4
09/26/2019	0.0.6	Preliminary Datasheet – Update 5 – Incorporated Additional Review Comments
10/24/2019	0.0.7	Preliminary Datasheet – Update 6 – Updated Package Drawings: Figs. 7.1-3
10/28/2019	0.0.8	Preliminary Datasheet – Pin List/Config.: Table 2.2 Updated; Table 2.3 Added
01/28/2020	0.0.9	Preliminary Datasheet – Part No. Changed to UT54LVDS454
02/18/2020	0.1.0	Preliminary Datasheet – Updates to Section 6 Electrical Parameters

Cobham Semiconductor Solutions – Datasheet Definitions

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Released Datasheet - Shipping QML & Reduced Hi – Rel

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

Cobham Semiconductor Solutions
4350 Centennial Blvd
Colorado Springs, CO 80907

COBHAM

E: info-ams@aeroflex.com
T: 800 645 8862

Aeroflex Colorado Springs Inc., dba Cobham Semiconductor Solutions, reserves the right to make changes to any products and services described herein at any time without notice. Consult Aeroflex or an authorized sales representative to verify that the information in this data sheet is current before using this product. Aeroflex does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing by Aeroflex; nor does the purchase, lease, or use of a product or service from Aeroflex convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual rights of Aeroflex or of third parties.