FEATURES
- 6702-EVAL for 100V input
- 6703-EVAL for 28V input
- 613140 iPOL included
- Output voltage 0.65V to 1.2V
- Output current to 50A

OPERATIONAL ENVIRONMENT
- Temperature Range: ambient only

APPLICATIONS
- Evaluation of IRM/iPOL performance and use

INTRODUCTION
The PDM series features an intermediate bus methodology of providing power. The IRM is responsible for providing the intermediate bus voltage and regulating it. This intermediate bus voltage is in the range of 26V to 48V and is designed to be a higher voltage so that it can be routed throughout a system with minimal concern to distribution losses. This intermediate bus voltage gets routed to the iPOL modules for voltage conversion and isolation (see Figure 1). The IRM is available with input voltages of 28V, 50V, 70V and 100V (the EVAL-6702 comes with a 100V converter, the EVAL-6703 comes with a 28V). The iPOL module is available with a voltage division ratio as high as 40 and efficient output current multiplying as high as 50A (both EVAL models come with a 613140 iPOL which is a divide by 40). Since the iPOL provides a fixed ratio voltage division, output voltages as low as 0.65V are capable.

With the use of the iPOL module large amounts of bulk capacitance is no longer required for large transient loads. The iPOL is an open loop device and the output is governed by the modules output impedance. Since the output impedance is very low and the iPOL is situated at the point-of-load, the transient response is very fast.

For full functionality and operation, it is recommended to operate both the IRM and iPOL together. However, it is possible to use the IRM alone as a non-isolated regulator. It is also possible to use the iPOL separately but, performance will be reduced without the IRM’s adaptive loop compensation.

The PDM Evaluation board includes all the flexibility needed to configure the IRM and the iPOL to demonstrate the modules performance. See Figure 2 to see a block diagram of the Evaluation board IRM and iPOL configuration features.

SAFETY PRECAUTIONS
During the operation of the evaluation board, high voltages may be utilized. Exhibit extreme caution when operating the evaluation board as it may lead to electrocution. Exercise extreme caution when connecting and disconnecting equipment as it could lead to inadvertent shorting or contact with a hot surface.
FUNCTIONAL DESCRIPTION

Required Equipment
The type of equipment required is application dependent. For instance, when using the 100V IRM, a supply capable of 100V is needed.

A recommended list of equipment can be seen below.

- Multiple power supplies if all modules are to be operated separately.
- A power supply capable of 100V @ 4A for (6702-EVAL) or 28V @ 6A for (6703-EVAL)
- A four channel oscilloscope
- Multiple DVMs
- Active load capable of doing 50A at <0.65V. Transient capable.
- Clip leads
- Alligator clips
- 8AWG wire or thicker to support high current output to active load
- Pliers
- Screwdrivers
- Small screw driver for adjusting potentiometers
- Appropriate module datasheets

Included Equipment
The included equipment with the evaluation kit includes the following items:

- Evaluation board populated with components
- Datasheets for Aeroflex components
- Evaluation board Application Note AN6702/03-EVAL
- Application Note ANPDM100
BOARD OVERVIEW
A picture of the PDM evaluation board can be seen below.

Refer to the number designated arrows above for the corresponding descriptions:

1) IRM board section (100V, 70V, 50V, 28V)
2) iPOL-1 Full Power Module board section
3) iPOL-2 Half Power Module board section
4) iPOL-3 Half Power Module board section
5) VRG8691/8692 Linear regulator board section
6) VRG8687/8688 Linear regulator board section
7) VRG8607/8608/8657/8658 Linear regulator board section
8) VRG8660/8662/8684 Linear regulator board section
9) VRG8666 Linear regulator board section
Refer to the number designated arrows above for the corresponding descriptions:

1) MIL-STD-461 Compliant EMI Filter for IRM
2) Board Revision
3) IRM Section
4) iPOL-1 Full Power Module board section
5) iPOL-2 Half Power Module board section
6) iPOL-3 Half Power Module board section
7) Linear regulator board section
IRM Pin Description and Test Points

The IRM board section contains various test points, switches, and potentiometers for evaluating the performance of the IRM.

Refer to the number designated arrows above for the corresponding descriptions:

1) **+In (PAD1)**: This is the IRM positive input voltage. Please be aware that the input voltage is dependent upon module model.
2) **–In (PAD2)**: This is this IRM input ground connection.
3) **IRM_TP1 (+In)**: This is a sense point for the positive input voltage to the IRM pin. Please note that this voltage is physically connected to the IRM’s +In pins. Refer to the evaluation board schematic for a diagram. Note that components exist between +In and the IRM +In pin as seen on the schematic diagram.
4) **Vin LED (D2)**: This is an LED indicator to show when an input voltage is applied to +In/-In. This should be removed for any efficiency measurements.
5) **BNC PC Probe Point (E1)**: This is a probe point for the PC input to the BNC and to the PC RC network. Note that this connection is floating when the PC Float switch is left in the floating position. Refer to the evaluation board schematic for a diagram.
6) **IRM TP2 (-In):** This is a sense point for the ground input to the IRM pin. Please note that this voltage is physically connected to the IRM’s –In pins. Refer to the evaluation board schematic for a diagram. Note that components exist between –In and the IRM –In pin as seen on the schematic diagram.

7) **PC BNC (P16):** This is a BNC connection meant to connect external inputs to control the PC pin on the IRM. The IRM voltage output is enabled when the PC pin is left open circuit (floating). To disable the IRM output voltage, the PC pin needs to be pulled low. Refer to the IRM datasheet for additional details about the PC pin. Note that the PC BNC is not directly connected to the IRM’s PC pin. Note that the PC Float switch must not be left in the float position for the BNC input to be connected to the IRM’s PC pin. Refer to the evaluation board schematic for a diagram.

8) **PC Adj Potentiometer (VR5):** This potentiometer is meant to control the RC time constant which determines the amount of time until the IRM’s output voltage is enabled.

9) **PC Switch (SW2):** This switch is meant to turn the output voltage of the IRM On or Off by either letting the PC pin float or pulling it to ground. Note that the PC Float Switch must not be in the float position or the PC switch will be isolated from the IRM’s PC pin.

10) **RG Adj Potentiometer (VR1):** This potentiometer is meant to adjust the amount of compensation provided on the output of the IRM to adapt to the output impedance of the iPOL. Refer to application note ANPDM100 for specifics on configuring the adaptive loop.

11) **OS Adj Potentiometer (VR2):** This potentiometer is meant to adjust the DC output voltage of the IRM.

12) **IL Adj Potentiometer (VR4):** This potentiometer is meant to adjust the DC current limit of the IRM.

13) **RG Sense Pin (P10):** This pin is directly connected to the IRM’s RG pin and is meant to read the voltage at the RG pin. It can also be used to measure the resistance of the RG Adj potentiometer.

14) **OS Sense Pin (P11):** This pin is directly connected to the IRM’s OS pin and is meant to read the voltage at the OS pin. It can also be used to measure the resistance of the OS Adj potentiometer.

15) **IL Switch (SW4):** This switch is meant to float the IL pin. This switch allows you to connect a fixed value from the IL Sense Pin to SG.

16) **IL Sense Pin (P14):** This pin is directly connected to the IRM’s IL pin and is meant to read the voltage at the IL pin.

17) **PC Float Switch (SW3):** This switch is meant to float the IRM’s PC pin so that it is isolated from the BNC PC input and the external RC network.

18) **PC Sense Pin (P15):** This pin is directly connected to the IRM’s PC pin and is meant to read the voltage at the PC pin.

19) **SG Probe Point (E2, E3):** This set of probe points is the signal ground. This is where all the measurements should be referenced to such as OS, RG, SC, TM and IL.

20) **RAL Adj Potentiometer (VR3):** This potentiometer is meant to adjust the amount of temperature compensation that is provided to the iPOL. Refer to application note ANPDM100 for specifics on configuring the adaptive loop. Note that this potentiometer on the IRM is best utilized as R_{AL1}.

21) **RAL IPOL Pin (P13):** This pin is meant to be connected to the iPOL’s RAL pin if temperature compensation is desired. If temperature compensation is not desired, it should be connected to SG as per application note ANPDM100.

22) **RAL Sense Pin (P12):** This pin is directly connected to the IRM’s RAL pin and is meant to be used to set the potentiometer value for the RAL Adj using the adjacent RAL iPOL pin.

23) **SG Probe Point (P9):** This is a binding post connected to the IRM’s signal ground pin.

24) **SC Float Switch (SW5):** This switch is meant to float the SC pin. This allows for an external capacitor to be used to connect to the SC probe point to the SG point.

25) **SC Probe Point (P8):** This pin is directly connected to the IRM’s SC pin and is meant to read the voltage at the SC pin. Refer to the IRM datasheet for additional details about the SC pin. Note that the SC pin is meant to control the rise time of the output voltage.

26) **PR Probe Point (P7):** This pin is directly connected to the IRM’s PR pin and is a mode of operation. However, this evaluation board does not cover the intended use of the PR pin since there is only one IRM available on this board. Refer to the IRM datasheet for additional details about the PR pin.

27) **VC Probe Point (P6):** This pin is directly connected to the IRM’s VC pin and is a mode of operation. Refer to the appropriate IRM and iPOL datasheet for using VC mode. Note that the UV pin needs to be floated on the iPOL for this mode of operation to work.
28) **TM Probe Point (P5):** This pin is directly connected to the IRM’s TM pin and is meant to read the voltage at the TM pin. The TM pin provides a voltage based upon the temperature of the IRM. At 27°C, the voltage at this pin is 2.00V +/-0.050V and changes 10mV/°C.

29) **IRM -Out (PAD3):** This is the IRM output ground. Refer to the appropriate IRM datasheet for a more detailed description about the –Out pin.

30) **IRM +Out (PAD4):** This is the IRM positive output voltage. Refer to the appropriate IRM datasheet for a more detailed description about the +Out pin. This provides the intermediate bus voltage for the ipOL modules.

31) **IRM Scope Sense (J1):** This is a probe point meant to fit an oscilloscope probe for observing the output of the IRM.

32) **VOut LED (D3):** This is an LED indicator to show when an output voltage is active on +Out/-Out. This should be removed for any efficiency measurements.

**IPOL PIN DESCRIPTION AND TEST POINTS**

The ipOL board sections contain various test points, switches, and potentiometers for evaluating the performance of the different types of ipOL modules.

Refer to the number designated arrows above for the corresponding descriptions:

1) **+In (PAD6):** This is the ipOL positive input voltage. This voltage is typically supplied from the IRM +Out but, can be externally supplied.

2) **–In (PAD8):** This is this ipOL input ground connection. This is typically connected to the IRM –Out.
3) **VC Probe Point** (P60): This pin is directly connected to the iPOL’s VC pin and is a mode of operation. Refer to the appropriate IRM and iPOL datasheet for using VC mode. Note that the UV pin needs to be floated on the iPOL for this mode of operation to work.

4) **–In Probe Point** (P61): This pin is connected to the iPOL’s –In pins. It is used as a reference point for the iPOL’s signals such as TM, UV, OV, etc.

5) **RAL Sense Pin** (P53): This pin is directly connected to the iPOL’s RAL pin and is meant to be used to set the potentiometer value for the RAL Adj using the adjacent RAL IRM pin.

6) **RAL IRM Pin** (P24): This pin is meant to be connected to the IRM’s SG pin if temperature compensation is desired. If temperature compensation is not desired, it should be left floating as per application note ANPDM100.

7) **RAL Adj Potentiometer** (VR17): This potentiometer is meant to adjust the amount of temperature compensation that is provided to the iPOL. Refer to application note ANPDM100 for specifics on configuring the adaptive loop. Note that this potentiometer on the iPOL is best utilized as \( R_{AL2} \).

8) **BNC PC Probe Point** (E8): This is a probe point for the PC input to the BNC and to the PC RC network. Note that this connection is floating when the PC Float switch is left in the floating position. Refer to the evaluation board schematic for a diagram.

9) **PC Adj Potentiometer** (VR18): This potentiometer is meant to control the RC time constant which determines the amount of time until the iPOL’s output voltage is enabled.

10) **PC Switch** (SW15): This switch is meant to turn the output voltage of the iPOL On or Off by either letting the PC pin float or pulling it to ground. Note that the PC Float Switch must not be in the float position or the PC switch will be isolated from the iPOL’s PC pin.

11) **PC Float Switch** (SW13): This switch is meant to float the iPOL’s PC pin so that it is isolated from the BNC PC input and the external RC network.

12) **UV Sense Pin** (P56): This pin is directly connected to the iPOL’s UV pin and is meant to read the voltage at the UV pin.

13) **PC Sense Pin** (P50): This pin is directly connected to the iPOL’s PC pin and is meant to read the voltage at the PC pin.

14) **iPOL TP1 (+In)**: This is a sense point for the positive input voltage to the iPOL pin. Please note that this voltage is physically connected to the iPOL’s +In pins. Refer to the evaluation board schematic for a diagram. Note that components may exist between +In and the iPOL’s +In pin as seen on the schematic diagram.

15) **–In Probe Point** (E13): This pin is connected to the iPOL’s –In pins. It is used as a reference point for the iPOL’s signals such as TM, UV, OV, etc.

16) **UV Adj Potentiometer** (VR19): This potentiometer is meant to adjust the point at which the iPOL trips due to an undervoltage. Refer to the iPOL datasheet for additional details on configuring the undervoltage point.

17) **UV Float Switch** (SW14): This switch is meant to float the iPOL’s UV pin so that VC mode can be evaluated. Refer to the iPOL datasheet for additional details on configuring VC mode.

18) **PC BNC** (P55): This is a BNC connection meant to connect external inputs to control the PC pin on the iPOL. The iPOL voltage output is enabled when the PC pin is left open circuit (floating). To disable the iPOL output voltage, the PC pin needs to be pulled low. Refer to the iPOL datasheet for additional details about the PC pin. Note that the PC BNC is not directly connected to the iPOL’s PC pin.

19) **UV Out Sense Pin** (P54): This pin is directly connected to the iPOL’s UV_Out pin and is meant to read the voltage at the UV_Out pin. Refer to the iPOL datasheet for additional details about the UV_Out pin.

20) **iPOL Scope Sense** (J2): This is a probe point meant to fit an oscilloscope probe for observing the output of the iPOL.

21) **iPOL -Out** (PAD7): This is the iPOL’s output ground. Refer to the appropriate iPOL datasheet for a more detailed description about the –Out pin.

22) **-IPOL +Out** (PAD5): This is the iPOL’s positive output voltage. Refer to the appropriate iPOL datasheet for a more detailed description about the +Out pin. This provides the high current iPOL output.

23) **VOut LED** (D5): This is an LED indicator to show when an output voltage is active on +Out/-Out. This should be removed for any efficiency measurements. Note that for low output voltages, this LED may not illuminate.

24) **iPOL TP3 (+Out)**: This is a sense point for the iPOL’s positive output voltage. Please note that this is directly connected as a kelvin sense point to the iPOL’s +Out pin. This should be used for making output impedance measurements and efficiency measurements.
25) **iPOL TP4 (-Out):** This is a sense point for the iPOL’s output ground. Please note that this is directly connected as a kelvin sense point to the iPOL’s -Out pin. This should be used for making output impedance measurements and efficiency measurements.

26) **OV Adj Potentiometer (VR20):** This potentiometer is meant to adjust the point at which the iPOL trips due to an overvoltage. Refer to the iPOL datasheet for additional details on configuring the overvoltage point.

27) **OV Float Switch (SW16):** This switch is meant to float the iPOL’s OV pin. This allows for easier adjustment of the overvoltage trip point.

28) **iPOL TP2 (-In):** This is a sense point for the ground input to the iPOL pin. Please note that this voltage is physically connected to the iPOL’s -In pins. Refer to the evaluation board schematic for a diagram. Note that components may exist between -In and the iPOL’s -In pin as seen on the schematic diagram.

29) **OV Sense Pin (P59):** This pin is directly connected to the iPOL’s OV pin and is meant to read the voltage at the OV pin.

30) **CLS Sense Pin (P57):** This pin is directly connected to the iPOL’s CLS pin and is meant to read the voltage at the CLS pin.

31) **CLS Adj Potentiometer (VR21):** This potentiometer is meant to adjust the DC current limit of the iPOL.

32) **–In Probe Point (E12,P62):** This pin is connected to the iPOL’s –In pins. It is used as a reference point for the iPOL’s signals such as TM, UV, OV, etc.

33) **TM Probe Point (P58):** This pin is directly connected to the iPOL’s TM pin and is meant to read the voltage at the TM pin. The TM pin provides a voltage based upon the temperature of the iPOL. At 27°C, the voltage at this pin is 2.00V +/-0.050V and changes 10mV/°C.

34) **Vin LED (D6):** This is an LED indicator to show when an input voltage is applied to +In/-In. This should be removed for any efficiency measurements.

**NOTE:** The following test procedure describes the testing of iRM module in conjunction with iPOL-1. In order to test other iPOLs (if installed) in the iPOL-2 & iPOL-3 locations, the same procedure can be followed by using the related designated switches, potentiometers and test terminals for the particular iPOL section. Please refer to Fig-6, Fig-7 and Table-3 for the list of corresponding designations for the particular iPOL.

**INITIAL SETUP**

1) Set IRM(U1) and IPOL-1(U2) switches according to Table-1 and Table-2.
2) Refer to Fig 5 for IRM/IPOL test setup.
3) Connect a short wire (Red) from IRM +Out(PAD4) to IPOL1 +In(PAD6). Connect a short wire (Blk) from IRM -Out(PAD3) to IPOL1 -In(PAD8). Do not connect jumper wire between P13 and P24 (Yellow wire) at this time.
4) Connect a Variable DC power supply to IRM input +In(PAD1) and –In(PAD2). Set the DC power supply to 0V and current limit to 4A.
5) Connect an Electronic load at the output of IPOL-1 PADS(+)+) and PAD7(-).
6) Connect a DVM at the output of IRM +Out(PAD4) and -Out(PAD3).
7) Connect a second DVM at the output of IPOL-1 voltage sense points **iPOL1_TP3(+)** and **iPOL1_TP4(-).**

**INITIAL STARTUP**

The IRM has a specification for input voltage rise time as per the IRM datasheet. It is recommended to slowly ramp the power supply voltage up to the accepted input voltage range dependent upon the installed IRM module. Please refer to the provided IRM datasheet for the proper input voltage (100V for 6702-EVAL or 28V for 6703-EVAL).

Please keep in mind that the iPOL modules provide fixed ratio voltages. The output voltage of the iPOL depends upon the input voltage. For instance, a K=1/40 iPOL with 40V of input provides a 1V output BEFORE any loading is added. If loading is added and the IRM is not configured to provide any adaptive loop compensation, the iPOL’s output voltage will be lower dependent upon the iPOL’s output impedance.

a) Slowly ramp up the input voltage to the IRM to proper level. When the input voltage is set, the DVM/scope should show a voltage between 26V to 48V on the output of the IRM.
b) Measure and verify the output voltage of the IRM and the iPOL module. Additionally, (if any linear post regulator is installed) then verify it’s output voltage.
c) Ramp up the load current to full load, on the output of iPOL-1. Make sure that both the IRM and iPOL-1 outputs can run with full load.
d) Power down the IRM input supply voltage.
NOTE: When testing the iPOL modules with an active load, make sure that the resistance in the cabling does not limit the amount of current that can be drawn from the module. I.e. Drawing 50A from a K=1/40 iPOL with 1V output requires that the wiring + termination resistance is less than 1V/50A = 20mOhm.

ADVANCED CONFIGURATIONS

1) **Changing the IRM Output Voltage**
   - a) Refer to the IRM datasheet for adjustment values for OS resistor for desired output voltage.
   - b) Adjust the potentiometer labelled OS_A (VR2) between the OS Sense Pin (P11) and any available SG pin (E2, E3) to the required OS resistance value.
   - c) Ramp UP the input supply voltage to the proper level.
   - d) Measure and verify the IRM and the iPOL output voltages. Please note that it is possible to set the IRM output voltage too high, in which case the overvoltage protection circuit will trip. The OS_A potentiometer will have to be reset to fix this condition.

2) **Changing the IRM Current Limit**
   Power down the IRM by removing the power from +In and -In. The IRM has a built in current limit trip point. If the external IL_A potentiometer (VR4) is set past the internal current limit trip point, the trip point will not exceed the factory default setting. Please note that the IRM current limit is factory set to ~ 3.0A.

   Refer to the IRM datasheet for a list of R_IL values for current limit. It should be noted that the IL pin of IRM has internal resistance of 4.99KΩ to SG. So, if the desired current limit is 1.50A which requires a recommended R_IL value of 4.32KΩ (for 100V IRM), then we must set the R_IL resistance to (4.32KΩ || 4.99KΩ) = 2.31KΩ.

   **NOTE:** For (28V IRM) we must set the R_IL resistance to (2.32KΩ || 4.99KΩ) = 1.58KΩ.

   - a) Measure resistance of R_IL from P14 to SG (E2, E3). Set R_IL to 2.31KΩ for (100V IRM) or 1.58KΩ for (28V IRM) by turning VR4 to set the IRM current limit to 1.50A.
   - b) Connect load to the IRM output IRM +Out(PAD4) and IRM -Out(PAD3).
   - c) Ramp up the input supply voltage to the IRM to proper level.
   - d) Ramp up the IRM load current past 1.50A trip point and verify the IRM output voltage collapses to 0, slightly above 1.50A load current.
   - e) Disable the load, and verify that the IRM output voltage recovers.
   - f) Power down the IRM input supply voltage.
   - g) Measure resistance of R_IL from P14 to SG (E2, E3). Set R_IL to 3.9KΩ for (100V IRM) or 2.8KΩ for (28V IRM) by turning VR4 to set the IRM current limit back to ~3.0A.
   - h) Ramp up the input supply voltage to the IRM to proper level.
   - i) Ramp up the IRM load current past 3.0A trip point and verify the IRM output voltage collapses to 0, slightly above 3.0A load current.
   - j) Disable the load, and verify that the IRM output voltage recovers.
   - k) Power down the IRM input supply voltage.
   - l) Disconnect load from the IRM output IRM +Out(PAD4) and IRM -Out(PAD3).
   - m) Connect load back to the iPOL-1 output iPOL +Out(PAD5) and iPOL -Out(PAD7).

3) **Configuring the Adaptive Loop**
   The Adaptive Loop is a feature of the IRM module which compensates for output voltage changes as the load current varies. These voltage changes are due to I*R voltage drops in the output resistance of the iPOL plus the PCB board trace resistance. With no load on the iPOL, the IRM is set to regulate the input voltage to the iPOL to produce the desired output voltage. Then, as more current is drawn by the load, the output voltage at the load will drop because voltage is lost across the output resistance of the iPOL and the PCB board trace resistance in accordance with Ohm’s Law. But as the iPOL load current increases, it is reflected from the iPOL output to the iPOL input, increasing the load current drawn from the IRM. The IRM senses this increase in load current and responds by slightly increasing the IRM output voltage to compensate for the resistive drop, which returns the load output voltage to its nominal value.

   Refer to the application note ANPDMIN100 for specifics on configuring the adaptive loop. The adaptive loop can only be used on one IRM/iPOL pair. The potentiometer provided by the IRM for RAL should be utilized as R_AL1 and the potentiometer located near the iPOL should be utilized as R_AL2.
The amount of compensation for the resistive drops is determined by RG resistor. Calculate the value of RG resistor by following the example given in the app note.

**NOTE:** Please note that the RG pin on IRM has approximately 6.22KΩ internal resistance to SG. It must be taken into account when setting the RG resistance. As an example, if the desired RG resistance is 20KΩ then we must set the resistance from RG pin to SG(E2, E3) to 4.7KΩ, (20KΩ || 6.22KΩ = 4.7KΩ).

a) Power down the IRM input supply voltage.
b) Measure resistance of RG from P10 to SG (E2, E3), set RG to 4.7KΩ by turning RGene_adj potentiometer VR1.
c) Connect a DVM in ohm meter setting between pin P12 & P13 in the iRM section and set RAL_IPOL resistance to 10KΩ by turning VR3.
d) Connect a DVM in ohm meter setting between pin P24 & P53 in the iPOL-1 section and set RAL_IRM resistance to 10KΩ by turning VR17.
e) Connect a DVM in Voltage mode setting at iRM output at PAD4(+) and PAD3(-).
f) Connect another DVM in Voltage mode setting at iPOL-1 output test points IPOL1_TP3(+) and IPOL1_TP4(-).
g) Disable the Electronic load connected to the iPOL-1 output.
h) Ramp up the input supply voltage to the iRM to proper level.
i) Set the iPOL-1 output voltage to 1.000V by slightly tweaking the iRM output voltage by turning OS_Adj potentiometer VR2 in the iRM section, with No load at the iPOL-1 output.
j) Power down the iRM input supply voltage.
k) Connect a jumper wire between RAL_IPOL pin P13 in IRM section and RAL_IRM pin P24 in iPOL-1 section. Please see Fig 5.
l) Ramp up the input supply voltage to the iRM to proper level.
m) Enable the Electronic load connected to the iPOL-1 output, and ramp up the load current to full load 50A.
n) Re-adjust VR3 in the iRM section and set the iPOL-1 output voltage to 1.000V with Full load 50A.
o) Disable the load and verify that there is very little change in IPOL-1 output voltage from Full load to No load.
p) Power down the iRM input supply voltage.

4) **Configuring VC Mode**

In VC mode, the IRM supplies a pulse for about 10mS to start the iPOL while the IRM ramps its output slowly from 0V. See the iPOL datasheet for a more detailed description on VC mode. Refer to the IRM and iPOL datasheet for the schematic for configuring VC mode.

First, make sure power is turned off on all the modules. Note that the IRM is only capable of starting up two iPOL modules in VC mode. Connect the IRM VC pin (P6) from the IRM to the VC pin (P60) of the iPOL-1 (a jumper wire may be already installed on the Evaluation Board).

In VC mode, the iPOL UV pin must be left floating. This can be accomplished by setting the UV Float Switch (SW14) on the iPOL-1 to UV_Float position.

In order to test the VC mode, do the following.

a) Power down the iRM input supply voltage.
b) Set the UV Float Switch (SW14) on the iPOL-1 to UV_Float position.
c) Connect Channel_1 (2V/div) of an oscilloscope to iRM_VC Pin (P6). Connect Channel_2 (0.5V/div) to the iPOL-1 output Scope Jack(J2). Connect scope GND to (P9 or P17) SG posts. Set Scope Horizontal sweep to 10ms/div. Trigger from Channel_1.
d) Enable the Electronic load connected to the iPOL-1 output and set it to 1.0A.
e) Ramp UP the iRM input supply voltage.
f) Observe the turn ON of the iPOL-1 output on Channel_2 with respect to the VC signal on Channel_1.
5) **Configuring PC Mode**

The IRM and iPOL PC mode can be configured as per the IRM and iPOL datasheets. In PC mode, the output voltage of the modules is Enabled when PC is left floating, and Disabled when PC is grounded. A PC On/Off switch is available on each IRM and iPOL module. Additionally, a PC Sense Pin and a BNC connection are available for sensing and external input control. An example of an external input control would be a signal from an Aeroflex Voltage Supervisor module for power sequencing. See the IRM and iPOL evaluation board sections for descriptions and usage of the PC On/Off Switch, the BNC PC Input, the PC Float Switch and the PC Sense Pin.

Another configurable parameter available on this evaluation kit for PC mode is the RC startup time constant. A potentiometer is available on all the IRM and iPOL modules called PC_Adj. Additionally, this can be disconnected by using the PC Float switch.

6) **PC ON/OFF Mode for the IRM**

In order to test the PC on/off mode for the IRM, do the following.

a) Power down the IRM input supply voltage.

b) Connect Channel_1 (1V/div) of an oscilloscope to IRM PC Sense Pin (P15). Connect Channel_2 (10V/div) to the IRM output Scope Jack(J1). Connect scope GND to (P9 or P17) SG posts. Set Scope Horizontal sweep to 10ms/div. Trigger from Channel_1.

c) Make sure PC_Float (SW3) switch is in Down/Close position.

d) Set IRM PC_Switch (SW2) to UP or OFF position.

e) Ramp up the input supply voltage to the IRM to proper level.

f) Set PC_Switch (SW2) to Down or ON position.

g) Observe the turn ON of the IRM output on Channel_2 with respect to the PC Enable signal on Channel_1.

7) **PC ON/OFF Mode for the IPOL**

In order to test the PC mode for the IPOL, do the following.

a) Power down the IRM input supply voltage.

b) Connect Channel_1 (1V/div) of an oscilloscope to iPOL PC Sense Pin (P50). Connect Channel_2 (0.5V/div) to the iPOL-1 output Scope Jack(J2). Connect scope GND to (P9 or P17) SG posts. Set Scope Horizontal sweep to 1ms/div. Trigger from Channel_1.

c) Enable the Electronic load connected to the iPOL-1 output and set it to 1.0A.

d) Set the UV Float Switch (SW14) on the iPOL-1 to Down/Close position.

e) Make sure iPOL-1 PC_Float (SW13) switch is in Down/Close position. Make sure that the IRM PC_Switch (SW2) is in Down or ON position.

f) Set IPOL-1 PC_Switch (SW15) to UP or OFF position.

g) Ramp up the input supply voltage to the IRM to proper level.

h) Set IPOL-1 PC_Switch (SW15) to Down or ON position.

i) Observe the turn ON of the iPOL-1 output on Channel_2 with respect to the PC Enable signal on Channel_1.

j) Power down the iRM input supply voltage.

**NOTE:** Alternatively, a (0 to 1.2V) step signal may be applied at the respective BNC PC (P16 or P55) Inputs to Enable and Disable the output, instead of using the manual PC_Switch.
8) **Configuring the iPOL Current Limit (CLS)**

The iPOL datasheet contains specifics about the Slow Current Limit (CLS). Typically, a 10KΩ resistor is installed to provide a current limit to about 133% of the iPOL’s rated output current. Increasing the CLS resistor above 10KΩ will lower the trip point for the iPOL module.

To adjust the current limit, the iPOL must be powered down. This can be done by disconnecting the power to the IRM. A CLS_Adj potentiometer is available to adjust iPOL current limit to the desired value. The value can be measured with a DVM from the CLS Sense pin to the nearest –In Probe point or SG.

For example, to decrease the current limit for iPOL-1 to about 35A, measure the resistance of CLS resistor on CLS_Sense Pin (P57) with respect to SG (E12 or E13) and set it to about 23KΩ by turning CLS_Adj Potentiometer (VR21) in iPOL-1 section.

After adjusting the potentiometer and removing the DVM, restore power and ramp up the iPOL-1 load current and verify that iPOL-1 current limit trips near 35A.

In order to restore full current capability of iPOL-1 set the CLS resistor on CLS_Sense Pin (P57) with respect to SG (E12 or E13) and set it to about 9.1KΩ by turning CLS_Adj potentiometer (VR21) in iPOL-1 section.

9) **Configuring the iPOL Overvoltage/Undervoltage**

The iPOL Undervoltage/Overvoltage functionality is described in the iPOL datasheet. A resistor divider is connected to the undervoltage and overvoltage pins. Typically, the trip point is at 1.2V on the iPOL’s UV and OV pins.

**NOTE:**

1) Please note that the top resistor for the divider on the Evaluation Board is 100KΩ which is different from the example given in the iPOL datasheet.

2) In order to test the OV and UV functionality of the iPOL, it may be necessary to disconnect the iPOL input from the IRM output, and connect the iPOL input to the variable DC input supply.

To adjust the overvoltage and undervoltage trip points, the iPOL must be powered down. This can be done by disconnecting the DC power supply from the input terminals of the IRM and connecting to the input terminals of the iPOL.

For iPOL, UV_Adj and OV_Adj potentiometers are available to adjust the UV/OV values to the desired levels. Since the potentiometers are in a divider network, calculations are required to determine the trip points. Refer to the iPOL datasheet for the calculations. Calculate the value of the bottom resistor for the desired UV and OV trip level.

The measurement for the potentiometers should be made from the UV Sense or OV Sense to the –In Probe point. Measure and adjust the UV_Adj and OV_Adj potentiometers for iPOL to the calculated value.

Remove the DVM, and slowly ramp up the input supply voltage to the iPOL without exceeding the maximum rated voltage, and observe the voltage at which the iPOL output turns ON (Undervoltage point).

Increase the input supply voltage to the iPOL further (do not exceed the maximum rated voltage for the iPOL input), and observe the voltage at which the iPOL output turns OFF (Overvoltage point).
10) **Undervoltage Test for the iPOL-1**

In order to test the Undervoltage for the **iPOL1**, do the following.
Assuming that the desired Undervoltage trip point is $V_{uv} = 26\, \text{V}$, calculate the value of Bottom resistor of the voltage divider by the following formula.

$$R_{bottom} = \left( \frac{1.2}{V_{uv} - 1.2} \right) \times 100\, \text{k}\Omega$$

$$R_{bottom} = \left( \frac{1.2}{26 - 1.2} \right) \times 100\, \text{k}\Omega = 4.84\, \text{k}\Omega$$

a) Disconnect iPOL-1 input from iRM output.
b) Connect the iPOL-1 input to the variable DC input supply.
c) Verify the **UV Float Switch** (SW14) on the iPOL-1 is in Down/Close position.
d) Connect a DVM in ohm meter setting between **UV Sense Pin** (P56) and $-\text{In}$ Probe point. Turn the **UV_Adj** (VR19) potentiometer and adjust the resistance value to 4.84KΩ.
e) Disconnect the DVM from **UV Sense Pin** (P56).
f) Connect **Channel_2** (0.5V/div) to the iPOL-1 output Scope Jack(J2). Set Scope Horizontal sweep to 10ms/div, Auto Trigger mode.
g) Enable the Electronic load connected to the iPOL-1 output and set it to 1.0A.
h) Slowly ramp up the input supply voltage to the iPOL-1 from 0 to 40V.
i) Observe the turn ON of the iPOL-1 output on Channel_2 when the input voltage reaches approximately 26V Undervoltage set point.
j) Power down the iPOL-1 input supply voltage to 0.

11) **Overvoltage Test for the iPOL-1**

In order to test the Overvoltage for the **iPOL-1**, do the following.
Assuming that the desired Overvoltage trip point is $V_{ov} = 50\, \text{V}$ calculate the value of Bottom resistor of the voltage divider by the following formula.

$$R_{bottom} = \left( \frac{1.2}{V_{ov} - 1.2} \right) \times 100\, \text{k}\Omega$$

$$R_{bottom} = \left( \frac{1.2}{50 - 1.2} \right) \times 100\, \text{k}\Omega = 2.45\, \text{k}\Omega$$

a) Disconnect iPOL-1 input from iRM output.
b) Connect the iPOL-1 input to the input supply.
c) Verify the **OV Float Switch** (SW16) on the iPOL-1 is in Up/Close position.
d) Connect a DVM in ohm meter setting between **OV Sense Pin** (P59) and $-\text{In}$ Probe point. Turn the **OV_Adj** (VR20) potentiometer and adjust the resistance value to 2.45KΩ.
e) Disconnect the DVM from **OV Sense Pin** (P59).
f) Connect **Channel_2** (0.5V/div) to the iPOL-1 output Scope Jack(J2). Set Scope Horizontal sweep to 10ms/div, Auto Trigger mode.
g) Enable the Electronic load connected to the iPOL-1 output and set it to 1.0A.
h) Slowly ramp up the input supply voltage to the iPOL-1 from 0 to 52V.
i) Observe the turn ON of the iPOL-1 output on Channel_2 when the input voltage reaches approximately 26V Undervoltage set point.
j) Slowly, continue ramping up the input voltage to the iPOL-1 to 52V. Observe the turn OFF of the iPOL-1 output on Channel_2 when the input voltage reaches approximately 50V Overvoltage set point.
k) Power down the iPOL-1 input supply voltage to 0.
### Table-1 Initial Settings for IRM (U1) SECTION

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>FUNCTION DESCRIPTION</th>
<th>SWITCH POSITION</th>
<th>MEASUREMENT POINTS</th>
<th>ADJ. VALUE</th>
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</thead>
<tbody>
<tr>
<td>SW2</td>
<td>PC ON/OFF</td>
<td>DOWN</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SW3</td>
<td>PC FLOAT</td>
<td>DOWN</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SW4</td>
<td>IRM IL</td>
<td>DOWN</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SW5</td>
<td>IRM SC</td>
<td>DOWN / CLOSE</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>VR1</td>
<td>R GENE ADJ.</td>
<td>-</td>
<td>P10, SG (E3)</td>
<td>4.7 KΩ</td>
</tr>
<tr>
<td>VR2</td>
<td>OUT VOLT ADJ.</td>
<td>-</td>
<td>P11, SG (E3)</td>
<td>2.8 KΩ (~40V)</td>
</tr>
<tr>
<td>VR3</td>
<td>RAL ADJ.</td>
<td>-</td>
<td>P12, P13</td>
<td>10 KΩ</td>
</tr>
<tr>
<td>VR4</td>
<td>I LIM ADJ.</td>
<td>-</td>
<td>P14, SG (E3)</td>
<td>3.9 KΩ (~3.0A for 100V iRM) 2.8 KΩ (~3.0A for 28V iRM)</td>
</tr>
<tr>
<td>VR5</td>
<td>PC ADJ.</td>
<td>-</td>
<td>E1, P15</td>
<td>&lt; 10 Ω</td>
</tr>
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### Table-2 Initial Settings for iPOL-1 (U2) SECTION

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<thead>
<tr>
<th>COMPONENT</th>
<th>FUNCTION DESCRIPTION</th>
<th>SWITCH POSITION</th>
<th>MEASUREMENT POINTS</th>
<th>ADJ. VALUE</th>
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<tr>
<td>SW13</td>
<td>PC</td>
<td>DOWN</td>
<td>-</td>
<td>-</td>
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<tr>
<td>SW14</td>
<td>UV</td>
<td>DOWN</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SW15</td>
<td>PC ON/OFF</td>
<td>PC ON</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SW16</td>
<td>OV</td>
<td>UP / CLOSE</td>
<td>-</td>
<td>-</td>
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<tr>
<td>VR17</td>
<td>RAL</td>
<td>-</td>
<td>P53, P24</td>
<td>10 KΩ</td>
</tr>
<tr>
<td>VR18</td>
<td>PC ADJ.</td>
<td>-</td>
<td>P50, E8</td>
<td>&lt; 10 Ω</td>
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<tr>
<td>VR19</td>
<td>UV ADJ.</td>
<td>-</td>
<td>P56, E12</td>
<td>4.84 KΩ (~26V)</td>
</tr>
<tr>
<td>VR20</td>
<td>OV ADJ.</td>
<td>-</td>
<td>P59, E12</td>
<td>2.45 KΩ (~50V)</td>
</tr>
<tr>
<td>VR21</td>
<td>CLS</td>
<td>-</td>
<td>P57, E12</td>
<td>9.16 KΩ</td>
</tr>
</tbody>
</table>
Figure 5 – IRM / IPOL Setup

POWER SUPPLY (100V @ 4A) for 6702-EVAL
or (28V @ 6A) for 6703-EVAL

TO IRM (U1) INPUT

IRM (U1) OUT TO IPOL-1 (U2)
INPUT JUMPERS

ELECTRONIC LOAD
- + TO IPOL-1 (U2)
OUTPUT

P13 to P24 Adaptive
Loop JumperWires

TO IRM (U1)
OUTPUT

KEITHLEY 2000 DVM #1

IPOL1 TP3(+)
IPOL1 TP4(-)

KEITHLEY 2000 DVM #2
FIGURE 6 – iPOL-2 Evaluation Board Section

If iPOL-2 is installed then refer to the number designated arrows above for the corresponding description in Table-3.
FIGURE 7 – iPOL-3 Evaluation Board Section

If iPOL-3 is installed then refer to the number designated arrows above for the corresponding description in Table-3.
<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>iPOL-1 (U2)</th>
<th>iPOL-2 (U3)</th>
<th>iPOL-3 (U4)</th>
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<tbody>
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<td>1</td>
<td>+In</td>
<td>PAD6</td>
<td>PAD10</td>
<td>PAD14</td>
</tr>
<tr>
<td>2</td>
<td>–In</td>
<td>PAD8</td>
<td>PAD12</td>
<td>PAD16</td>
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<td>3</td>
<td>VC Probe Point</td>
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<td>–In Probe Point</td>
<td>P61</td>
<td>P77</td>
<td>P93</td>
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<tr>
<td>5</td>
<td>RAL Sense Pin</td>
<td>P53</td>
<td>P69</td>
<td>P84</td>
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<td>6</td>
<td>RAL IRM Pin</td>
<td>P24</td>
<td>P68</td>
<td>P83</td>
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<td>7</td>
<td>RAL Adj Potentiometer</td>
<td>VR17</td>
<td>VR22</td>
<td>VR27</td>
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<tr>
<td>8</td>
<td>BNC PC Probe Point</td>
<td>E8</td>
<td>E14</td>
<td>E20</td>
</tr>
<tr>
<td>9</td>
<td>PC Adj Potentiometer</td>
<td>VR18</td>
<td>VR23</td>
<td>VR28</td>
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<tr>
<td>10</td>
<td>PC Switch</td>
<td>SW15</td>
<td>SW20</td>
<td>SW26</td>
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<tr>
<td>11</td>
<td>PC Float Switch</td>
<td>SW13</td>
<td>SW18</td>
<td>SW24</td>
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<tr>
<td>12</td>
<td>UV Sense Pin</td>
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<td>P72</td>
<td>P88</td>
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<td>PC Sense Pin</td>
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<td>P63</td>
<td>P78</td>
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<tr>
<td>14</td>
<td>iPOL_T1 (+)</td>
<td>iPOL1_T1</td>
<td>iPOL2_T1</td>
<td>iPOL3_T1</td>
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<tr>
<td>15</td>
<td>–In Probe Point</td>
<td>E13</td>
<td>E15</td>
<td>E25</td>
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<tr>
<td>16</td>
<td>UV Adj Potentiometer</td>
<td>VR19</td>
<td>VR24</td>
<td>VR29</td>
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<tr>
<td>17</td>
<td>UV Float Switch</td>
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<td>SW25</td>
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<td>PC IN BNC_1</td>
<td>PC IN BNC_2</td>
<td>PC IN BNC_3</td>
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<td>UV Out Sense Pin</td>
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<td>iPOL Scope Sense</td>
<td>J2</td>
<td>J3</td>
<td>J4</td>
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<td>iPOL –Out</td>
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<td>PAD11</td>
<td>PAD15</td>
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<tr>
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<td>iPOL +Out</td>
<td>PAD5</td>
<td>PAD9</td>
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<td>VOut LED</td>
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<td>D8</td>
<td>D11</td>
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<td>iPOL_T4 (-)</td>
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<td>iPOL3_T4</td>
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<tr>
<td>26</td>
<td>OV_Adj Potentiometer</td>
<td>VR20</td>
<td>VR25</td>
<td>VR30</td>
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<td>SW16</td>
<td>SW21</td>
<td>SW27</td>
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<td>iPOL_T2 (-)</td>
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<td>P74</td>
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<td>CLS Sense Pin</td>
<td>P57</td>
<td>P71</td>
<td>P87</td>
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<td>CLS Adj Potentiometer</td>
<td>VR21</td>
<td>VR26</td>
<td>VR31</td>
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<tr>
<td>32</td>
<td>–In Probe Point</td>
<td>E12, P62</td>
<td>E18, P76</td>
<td>E24, P92</td>
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<td>33</td>
<td>TM Probe Point</td>
<td>P58</td>
<td>P73</td>
<td>P89</td>
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<td>34</td>
<td>Vin LED</td>
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<td>D9</td>
<td>D12</td>
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ORDERING INFORMATION

Generic Datasheet Part Numbering

67XX-EVAL

PDM EVAL BOARD

100V Input (6702-EVAL)
28V Input (6703-EVAL)
## REVISION HISTORY

<table>
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<th>Change Description</th>
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**Cobham Semiconductor Solutions – Datasheet Definitions**

*Advanced Datasheet - Product In Development*

*Preliminary Datasheet - Shipping Prototype*

*Released Datasheet - Shipping QML & Reduced Hi – Rel*

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