Overview

The GEN 6 LEON 3FT Single Board Computer (SBC) is Cobham Semiconductor Solutions’ (formerly Aeroflex) Flight Ready TRL-6 based, off the shelf system designed for LEO, GEO, and Planetary command and control applications. The board is designed with a flexible core architecture to balance power and performance needs. The system is capable of up to 95 Dhrystone MIPS with a 132MHz System Clock.

The GEN 6 SBC is equipped with 64MB of EDAC protected SRAM and 32MB of EDAC protected Non-Volatile Memory. There are 3 physical interface types on the SBC: cPCI, SpaceWire and a test and development interface. The cPCI interface connectors support 32 bit 33MHz PCI bus as well as 1553B, SPI, and CAN. The 1553B, SPI and CAN interfaces are implemented via unused signals of the J2 cPCI connector. The test and development interface is a 37 pin MDM connector that supports access to the LEON 3FT Debug Support Unit (DSU), Ethernet, and processor reset via the Cobham supplied Interface Pod. The SBC comes with an additional Interface Pod to expand the capabilities and debug/software loading of the GEN 6 SBC.
System Synchronized Multi-Frequency Clock Network Management System

The GEN 6 SBC is capable of managing power and performance by configuring board components to run clock frequencies that are ideal for a particular user application. There are five available configurations offering different performance in regard to speed, throughput, and power. Thus, users can choose a configuration tailored to their particular power and performance needs when using the GEN 6 SBC. The following table demonstrates the possible configurations:

<table>
<thead>
<tr>
<th>CPU Version</th>
<th>CPU Clock</th>
<th>SpaceWire Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>UT700</td>
<td>33MHz</td>
<td>33MHz</td>
</tr>
<tr>
<td>UT700</td>
<td>66MHz</td>
<td>132MHz</td>
</tr>
<tr>
<td>UT700</td>
<td>132MHz</td>
<td>132MHz</td>
</tr>
<tr>
<td>UT699E</td>
<td>33MHz</td>
<td>33MHz</td>
</tr>
<tr>
<td>UT699E</td>
<td>66MHz</td>
<td>132MHz</td>
</tr>
</tbody>
</table>

Expandable Digital IO Capabilities

The GEN 6 SBC is capable of supporting additional signal types by connecting to 8 spare signal pins on the cPCI J2 connector on the SBC backplane. Users who need to process signal types outside the integrated feature set can construct a simple expander card that attaches to these 8 pins to drive those signal types across the SBC, allowing for extensibility to applications outside its base feature set.
**J3 Interface Pod**

The GEN 6 includes an Interface Pod designed to enable Ethernet, Serial DSU, and UART functionality on the SBC. The Pod interfaces to the GEN 6 SBC via the test and development interface connector as shown in Figure 3. A PC can be used to interface through mini USB and RJ45 Ethernet connectors to J3 on the SBC, giving users the ability to run GRMON which allows the capability of loading and running software, testing the Ethernet interface or even setting up an OS interface such as VxWorks.

![J3 Interface Pod Diagram](image)

**Figure 3. J3 Interface Pod Configuration and Board Layout.**

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