FEATURES

- Programmable, read-only, asynchronous, radiation-hardened, 8K x 8 memory
  - Supported by industry standard programmer
- 35ns and 45ns maximum address access time (-55 °C to +125 °C)
- TTL compatible input and TTL/CMOS compatible output levels
- Three-state data bus
- Low operating and standby current
  - Operating: 100mA maximum @28.6MHz
    - Derating: 3mA/MHz
  - Standby: 500µA maximum (post-rad)
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - Total dose: 1E6 rad(Si)
  - LET_{TH}(0.25) ~ 100 MeV-cm^2/mg
  - SEL Immune ≥128 MeV-cm^2/mg
  - Saturated Cross Section cm^2 per bit, 1.0E-11
    - 1.2E-8 errors/device-day, Adams 90% geosynchronous heavy ion
- Memory cell LET threshold: >128 MeV-cm^2/mg
- QML Q & V compliant part
  - AC and DC testing at factory
- Packaging options:
  - 28-pin 100-mil center DIP (0.600 x 1.4)
  - 28-lead 50-mil center flatpack (0.490 x 0.74)
- V_{DD}: 5.0 volts ± 10%
- Standard Microcircuit Drawing 5962-96873

PRODUCT DESCRIPTION

The UT28F64 amorphous silicon anti-fuse PROM is a high performance, asynchronous, radiation-hardened, 8K x 8 programmable memory device. The UT28F64 PROM features fully asynchronous operation requiring no external clocks or timing strobes. An advanced radiation-hardened twin-well CMOS process technology is used to implement the UT28F64. The combination of radiation-hardness, fast access time, and low power consumption make the UT28F64 ideal for high speed systems designed for operation in radiation environments.
DEVICE OPERATION

The UT28F64 has three control inputs: Chip Enable (CE), Program Enable (PE), and Output Enable (OE); thirteen address inputs, A(12:0); and eight bidirectional data lines, DQ(7:0). CE is the device enable input that controls chip selection, active, and standby modes. Asserting CE causes I_{DD} to rise to its active value and decodes the thirteen address inputs to select one of 8,192 words in the memory. PE controls program and read operations. During a read cycle, OE must be asserted to enable the outputs.

PIN NAMES

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A(12:0)</td>
<td>Address</td>
</tr>
<tr>
<td>CE</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>OE</td>
<td>Output Enable</td>
</tr>
<tr>
<td>PE</td>
<td>Program Enable</td>
</tr>
<tr>
<td>DQ(7:0)</td>
<td>Data Input/Data Output</td>
</tr>
</tbody>
</table>

PIN CONFIGURATION

| NC | 1 | 28 | V_{DD} |
| A12 | 2 | 27 | PE |
| A7 | 3 | 26 | NC |
| A6 | 4 | 25 | A8 |
| A5 | 5 | 24 | A9 |
| A4 | 6 | 23 | A11 |
| A3 | 7 | 22 | OE |
| A2 | 8 | 21 | A10 |
| A1 | 9 | 20 | CE |
| A0 | 10 | 19 | DQ7 |
| DQ0 | 11 | 18 | DQ6 |
| DQ1 | 12 | 17 | DQ5 |
| DQ2 | 13 | 16 | DQ4 |
| V_{SS} | 14 | 15 | DQ3 |

ABSOLUTE MAXIMUM RATINGS

(Referenced to V_{SS})

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD}</td>
<td>DC supply voltage</td>
<td>-0.3 to 7.0</td>
<td>V</td>
</tr>
<tr>
<td>V_{IO}</td>
<td>Voltage on any pin</td>
<td>-0.5 to (V_{DD} + 0.5)</td>
<td>V</td>
</tr>
<tr>
<td>T_{STG}</td>
<td>Storage temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>P_{D}</td>
<td>Maximum power dissipation</td>
<td>1.5</td>
<td>W</td>
</tr>
<tr>
<td>T_{J}</td>
<td>Maximum junction temperature</td>
<td>+175</td>
<td>°C</td>
</tr>
<tr>
<td>Θ_{JC}</td>
<td>Thermal resistance, junction-to-case</td>
<td>3.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>I_{I}</td>
<td>DC input current</td>
<td>±10</td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012, infinite heat sink.
**RECOMMENDED OPERATING CONDITIONS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DD</td>
<td>Positive supply voltage</td>
<td>4.5 to 5.5V</td>
<td>V</td>
</tr>
<tr>
<td>T_C</td>
<td>Case temperature range</td>
<td>-55 to +125°C</td>
<td>°C</td>
</tr>
<tr>
<td>V_IN</td>
<td>DC input voltage</td>
<td>0 to V_DD</td>
<td>V</td>
</tr>
</tbody>
</table>

**DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(V_DD = 5.0V ±10%; -55°C < T_C < +125°C)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_PP</td>
<td>High-level input voltage</td>
<td>(TTL)</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_SSL</td>
<td>Low-level input voltage</td>
<td>(TTL)</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_OPL</td>
<td>Low-level output voltage</td>
<td>IOL = 4.8mA, V_DD = 4.5V (TTL)</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_OPL2</td>
<td>Low-level output voltage</td>
<td>IOL = 200µA, V_DD = 4.5V (CMOS)</td>
<td>VSS + 0.05</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_OPH1</td>
<td>High-level output voltage</td>
<td>IOH = -400µA, V_DD = 4.5V (TTL)</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_OPH2</td>
<td>High-level output voltage</td>
<td>IOH = -200µA V_DD = 4.5V (CMOS)</td>
<td>4.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>C_IN</td>
<td>Input capacitance</td>
<td>f = 1MHz, V_DD = 5.0V</td>
<td>15</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>C_IO</td>
<td>Bidirectional I/O capacitance</td>
<td>f = 1MHz, V_DD = 5.0V</td>
<td>15</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>I_IN</td>
<td>Input leakage current</td>
<td>V_IN = 0V to V_DD</td>
<td>-1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I_OZ</td>
<td>Three-state output leakage current</td>
<td>V_O = 0V to V_DD</td>
<td>10</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I_OSS</td>
<td>Short-circuit output current</td>
<td>V_DD = 5.5V, V_O = V_DD</td>
<td>-90</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_DDOP</td>
<td>Supply current operating @28.6MHz (35ns product)</td>
<td>TTL input levels (I_OUT = 0), V_IL = 0.2V</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>@22.2MHz (45ns product)</td>
<td>V_DD = 5.5V, V_O = 0V</td>
<td>85</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_DDSB</td>
<td>Supply current standby CMOS input levels ,</td>
<td>V_IL = V_SS to 0.25V</td>
<td>500</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>post-rad</td>
<td>V_CE = V_DD -0.25, V_IH = V_DD -0.25</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
5. Derates at 2.5mA/MHz.
READ CYCLE

A combination of $\overline{PE}$ greater than $V_{IH}(\text{min})$, and $\overline{CE}$ less than $V_{IL}(\text{max})$ defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

An address access read is initiated by a change in address inputs while the chip is enabled with $\overline{OE}$ asserted and $\overline{PE}$ deasserted. Valid data appears on data output, DQ(7:0), after the specified $t_{AVQV}$ is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time.

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*
($V_{DD} = 5.0\text{V} \pm 10\%; -55^\circ\text{C} < T_C < +125^\circ\text{C}$)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>28F64-35 MIN</th>
<th>28F64-35 MAX</th>
<th>28F64-45 MIN</th>
<th>28F64-45 MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{AVAV}^1$</td>
<td>Read cycle time</td>
<td>35</td>
<td>45</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AVQV}$</td>
<td>Read access time</td>
<td></td>
<td></td>
<td>35</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AXQX}^2$</td>
<td>Output hold time</td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{GLQX}^2$</td>
<td>$\overline{OE}$-controlled output enable time</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{GLQV}$</td>
<td>$\overline{OE}$-controlled access time</td>
<td></td>
<td></td>
<td>15</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{GHQZ}$</td>
<td>$\overline{OE}$-controlled output three-state time</td>
<td>15</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ELQX}^2$</td>
<td>$\overline{CE}$-controlled output enable time</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ELQV}$</td>
<td>$\overline{CE}$-controlled access time</td>
<td></td>
<td></td>
<td>35</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{EHQZ}$</td>
<td>$\overline{CE}$-controlled output three-state time</td>
<td>15</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
1. Functional test.
2. Three-state is defined as a 400mV change from steady-state output voltage.

The chip enable-controlled access is initiated by $\overline{CE}$ going active while $\overline{OE}$ remains asserted, $\overline{PE}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified $t_{ELQV}$ is satisfied, the eight-bit word addressed by $A(12:0)$ appears at the data outputs DQ(7:0).

Output enable-controlled access is initiated by $\overline{OE}$ going active while $\overline{CE}$ is asserted, $\overline{PE}$ is deasserted, and the addresses are stable. Read access time is $t_{GLQV}$ unless $t_{AVQV}$ or $t_{ELQV}$ have not been satisfied.
RADIATION HARDNESS

The UT28F64 PROM incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose</td>
<td>5.0E5 rad(Si)</td>
</tr>
<tr>
<td>Latchup LET Threshold</td>
<td>&gt;128 MeV·cm²/mg</td>
</tr>
<tr>
<td>Memory Cell LET Threshold</td>
<td>&gt;128 MeV·cm²/mg</td>
</tr>
<tr>
<td>Transient Upset LET Threshold</td>
<td>54 MeV·cm²/mg</td>
</tr>
<tr>
<td>Transient Upset Device Cross Section @ LET=128 MeV·cm²/mg</td>
<td>1E-6 cm²</td>
</tr>
</tbody>
</table>

Note:
1. The PROM will not latchup during radiation exposure under recommended operating conditions.
Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (TTL input = 1.5V).

**Figure 3. AC Test Loads and Input Waveforms**
Notes:
1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-PRF-38535.
3. Ceramic to be opaque.

Figure 4. 28-Pin 100-mil Center DIP (0.600 x 1.4)
Notes:
1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to \( V_{SS} \).
3. Lead finishes are in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option.
7. With solder, increase maximum by 0.003.

**Figure 5.** 28-Lead 50-mil Center Flatpack (0.490 x 0.74)
ORDERING INFORMATION

64K PROM: SMD

5962 * 96873 *

Lead Finish:
(A) = Solder
(C) = Gold
(X) = Optional

Case Outline:
(X) = 28-pin DIP
(Y) = 28-lead Flatpack

Class Designator:
(Q) = Class Q
(V) = Class V

Device Type
(01) = 35ns Access Time, TTL inputs, CMOS/TTL compatible outputs
(02) = 45ns Access Time, TTL inputs, CMOS/TTL compatible outputs

Drawing Number: 96873

Total Dose:
(G) = 5E5 rads(Si)
(F) = 3E5 rads(Si)
(R) = 1E5 rads(Si)
(H) = 1E6 rads(Si)

Federal Stock Class Designator: No options

Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.
4. Lead finish: Factory programming either solder or gold. Field programming gold only.
## 64K PROM

<table>
<thead>
<tr>
<th>UT</th>
<th>****</th>
<th>*</th>
<th>*</th>
<th>*</th>
<th>*</th>
<th>*</th>
</tr>
</thead>
</table>

**Total Dose:**
- ( ) = None

**Lead Finish:**
- (A) = Solder
- (C) = Gold
- (X) = Optional

**Screening:**
- (C) = Mil Temp
- (P) = Prototype

**Package Type:**
- (P) = 28-lead DIP
- (U) = 28-lead Flatpack

**Access Time:**
- (35) = 35ns access time, TTL compatible inputs, CMOS/TTL compatible outputs
- (45) = 45ns access time, TTL compatible inputs, CMOS/TTL compatible outputs

**Device Type Modifier:**
- (T) = TTL compatible inputs and CMOS/TTL compatible outputs

**Device Type:**
- (28F64) = 8Kx8 One Time Programmable PROM

### Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an “X” is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
4. Prototype flow per UTMC Manufacturing Flows Document. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is gold only.
5. Lead finish: Factory programming either solder or gold. Field programming gold only.
Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development
Preliminary Datasheet - Shipping Prototype
Datasheet - Shipping QML & Reduced Hi-Rel

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused.

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