FEATURES

- Programmable, read-only, asynchronous, radiation-hardened, 32K x 8 memory
  - Supported by industry standard programmer
  - Programming yield estimated at 80% or greater (ref note on ordering page(s))
- 45ns maximum address access time (-55°C to +125°C)
- TTL compatible input and TTL/CMOS compatible output levels
- Three-state data bus
- Low operating and standby current
  - Operating: 80mA maximum @25MHz
  - Derating: 3mA/MHz
  - Standby: 1.5mA maximum (post-rad)
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - Total dose: 100Krad to 1Megarad(Si)
  - Onset LET: 57 MeV-cm²/mg
  - SEL Immune ≥110 MeV-cm²/mg
- QML Q & V compliant part
  - AC and DC testing at factory
- No post program conditioning
- Packaging options:
  - 28-lead 50-mil center flatpack (0.490 x 0.74)
- VDD: 5.0 volts ± 10%
- Standard Microcircuit Drawing 5962-96891

PRODUCT DESCRIPTION

The UT28F256QLE amorphous silicon redundant ViaLink™ PROM is a high performance, asynchronous, radiation-hardened, 32K x 8 programmable memory device. The UT28F256QLE PROM features fully asynchronous operation requiring no external clocks or timing strobes. An advanced radiation-hardened twin-well CMOS process technology is used to implement the UT28F256QLE. The combination of radiation-hardness, fast access time, and low power consumption make the UT28F256QLE ideal for high speed systems designed for operation in radiation environments.

Figure 1. PROM Block Diagram
DEVICE OPERATION

The UT28F256QLE has three control inputs: Chip Enable (CE), Program Enable (PE), and Output Enable (OE); fifteen address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). CE is the device enable input that controls chip selection, active, and standby modes. Asserting CE causes IDD to rise to its active value and decodes the fifteen address inputs to select one of 32,768 words in the memory. PE controls program and read operations. During a read cycle, OE must be asserted to enable the outputs.

PIN NAMES

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A(14:0)</td>
<td>Address</td>
</tr>
<tr>
<td>CE</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>OE</td>
<td>Output Enable</td>
</tr>
<tr>
<td>PE</td>
<td>Program Enable</td>
</tr>
<tr>
<td>DQ(7:0)</td>
<td>Data Input/Data Output</td>
</tr>
</tbody>
</table>

Table 1. Device Operation Truth Table

<table>
<thead>
<tr>
<th>OE</th>
<th>PE</th>
<th>CE</th>
<th>I/O MODE</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Data Out</td>
<td>Read</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Data In</td>
<td>Program</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Three-state</td>
<td>Read</td>
</tr>
</tbody>
</table>

Notes:
1. “X” is defined as a “don’t care” condition.
2. Device active; outputs disabled.

PIN CONFIGURATION

<table>
<thead>
<tr>
<th>A14</th>
<th>A12</th>
<th>A7</th>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>DQ0</th>
<th>DQ1</th>
<th>DQ2</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>28</td>
<td>2</td>
<td>27</td>
<td>3</td>
<td>26</td>
<td>4</td>
<td>25</td>
<td>5</td>
<td>24</td>
<td>6</td>
<td>23</td>
<td>7</td>
<td>22</td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS

(Referenced to VSS)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>DC supply voltage</td>
<td>-0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>Voltage on any pin</td>
<td>-0.5 to (VDD + 0.5)</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>PD</td>
<td>Maximum power dissipation</td>
<td>1.5</td>
<td>W</td>
</tr>
<tr>
<td>TJ</td>
<td>Maximum junction temperature</td>
<td>+175</td>
<td>°C</td>
</tr>
<tr>
<td>JJC</td>
<td>Thermal resistance, junction-to-case</td>
<td>3.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>I1</td>
<td>DC input current</td>
<td>±10</td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012, infinite heat sink.
RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Positive supply voltage</td>
<td>4.5 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>TC</td>
<td>Case temperature range</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>VIN</td>
<td>DC input voltage</td>
<td>0 to VDD</td>
<td>V</td>
</tr>
</tbody>
</table>

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

\( V_{DD} = 5.0V \pm 10\%; -55^\circ C < T_C < +125^\circ C \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High-level input voltage</td>
<td>(TTL)</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Low-level input voltage</td>
<td>(TTL)</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OL1}</td>
<td>Low-level output voltage</td>
<td>( I_{OL} = 4.0mA, V_{DD} = 4.5V ) (TTL)</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OL2}</td>
<td>Low-level output voltage</td>
<td>( I_{OL} = 200\mu A, V_{DD} = 4.5V ) (CMOS)</td>
<td>( V_{SS} + 0.10 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OH1}</td>
<td>High-level output voltage</td>
<td>( I_{OH} = -200\mu A, V_{DD} = 4.5V ) (CMOS)</td>
<td>( V_{DD} -0.1 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OH2}</td>
<td>High-level output voltage</td>
<td>( I_{OH} = -2.0mA, V_{DD} = 4.5V ) (TTL)</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>C_{IN}</td>
<td>Input capacitance , all inputs except PE</td>
<td>( f = 1MHz, V_{DD} = 5.0V ) ( V_{IN} = 0V )</td>
<td>15</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{IO}</td>
<td>Bidirectional I/O capacitance</td>
<td>( f = 1MHz, V_{DD} = 5.0V ) ( V_{OUT} = 0V )</td>
<td>15</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>I_{IN}</td>
<td>Input leakage current</td>
<td>( V_{IN} = 0V ) to ( V_{DD} ), all pins except PE ( V_{IN} = V_{DD}, PE ) only</td>
<td>-5</td>
<td>+5</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>I_{OZ}</td>
<td>Three-state output leakage current</td>
<td>( V_O = 0V ) to ( V_{DD} ) ( V_{DD} = 5.5V ) ( OE = 5.5V )</td>
<td>-10</td>
<td>+10</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>I_{OS}</td>
<td>Short-circuit output current</td>
<td>( V_{DD} = 5.5V, V_O = V_{DD} ) ( V_{DD} = 5.5V, V_O = 0V )</td>
<td>-120</td>
<td>120</td>
<td>mA</td>
</tr>
<tr>
<td>I_{DD1(OP)}</td>
<td>Supply current operating ( @22.2MHz ) (45ns product)</td>
<td>TTL inputs levels ( (I_{OUT} = 0), V_{IL} = 0.2V ) ( V_{DD}, PE = 5.5V )</td>
<td>80</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I_{DD2(SB)}</td>
<td>Supply current standby</td>
<td>CMOS input levels ( V_{IL} = V_{SS} +0.25V ) ( C_E = V_{DD} - 0.25 V_{IH} = V_{DD} - 0.25V )</td>
<td>1.5</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1E6 rad(Si).
1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Derates at 3.2mA/MHz.
READ CYCLE

A combination of PE greater than \( V_{IH}(\text{min}) \), and CE less than \( V_{IL}(\text{max}) \) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

An address access read is initiated by a change in address inputs while the chip is enabled with OE asserted and PE deasserted. Valid data appears on data output, \( DQ(7:0) \), after the specified \( t_{AVQV} \) is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time.

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

\( (V_{DD} = 5.0V \pm 10\%; -55^\circ C < T_C < +125^\circ C) \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>28F256-45 MIN</th>
<th>28F256-45 MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{AVAV} )</td>
<td>Read cycle time</td>
<td>45</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AVQV} )</td>
<td>Read access time</td>
<td></td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AXQX} )</td>
<td>Output hold time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{GLQX} )</td>
<td>( \overline{OE} )-controlled output enable time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{GLQV} )</td>
<td>( \overline{OE} )-controlled access time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{GHQZ} )</td>
<td>( \overline{OE} )-controlled output three-state time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{ELQX} )</td>
<td>( \overline{CE} )-controlled output enable time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{ELQV} )</td>
<td>( \overline{CE} )-controlled access time</td>
<td>45</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{EHQZ} )</td>
<td>( \overline{CE} )-controlled output three-state time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
1. Functional test.
2. Three-state is defined as a 200mV change from steady-state output voltage.
RADIATION HARDNESS

The UT28F256QLE PROM incorporates special design and layout features which allow operation in high-level radiation environments. Aeroflex Colorado Springs has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dose</td>
<td>1E6 rad(Si)</td>
</tr>
<tr>
<td>Latchup LET Threshold</td>
<td>&gt;110 MeV-cm²/mg</td>
</tr>
<tr>
<td>Memory Cell LET Threshold</td>
<td>&gt;100 MeV-cm²/mg</td>
</tr>
<tr>
<td>Logic Onset LET</td>
<td>&gt;57 MeV-cm²/mg</td>
</tr>
<tr>
<td>SEU Cross Section</td>
<td>9.4E-7 cm²/device</td>
</tr>
<tr>
<td>Error rate - geosynchronous orbit, Adams 90% worst case environment</td>
<td>5.1E-15 errors/device day</td>
</tr>
</tbody>
</table>

Note:
1. The PROM will not latchup during radiation exposure under recommended operating conditions.
Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (TTL input = 1.5V).

Figure 3. AC Test Loads and Input Waveforms
Figure 5. 28-Lead 50-mil Center Flatpack (0.490 x 0.74)

Notes:
1. All exposed metalized areas to be plated per MIL-PRF-38535.
2. The lid is connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option.
7. With solder, increase maximum by 0.003.
8. Total weight is approximately 2.4 grams.
ORDERING INFORMATION

256KQLE PROM: SMD

5962 * 96891 *

Lead Finish:
(A) = Solder
(C) = Gold
(X) = Optional

Case Outline:
(X) = 28-lead Flatpack

Class Designator:
(Q) = Class Q
(V) = Class V

Device Type
(09) = 45ns Access Time, TTL inputs, CMOS/TTL compatible outputs
(10) = 45ns Access Time, TTL inputs, CMOS/TTL compatible outputs Extended Industrial Temp
(-40°C to +125°C)

Drawing Number: 96891

Total Dose:
(F) = 3E5 rads(Si)
(G) = 5E5 rads(Si)
(H) = 1E6 rads(Si)
(R) = 1E5 rads(Si)

Federal Stock Class Designator: No options

Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.
4. Device type 09 available with total dose of 1E5 rads(Si) or 3E5 rads(Si).
5. Due to the unique nature of field programmed devices, Cobham does not guarantee program yield or accept returns for programming failures. Cobham estimates programming yield at 80% or greater. Users should reference the “QLE Programming Guide” and the "QLE Programming Notes" documents available under the Applications Notes tab of the Cobham HiRel Microelectronics Memory device webpage for programming instructions and information.
256KQLE PROM

UT   ****   *   - *    *   *   *   *

Total Dose:
( ) = None

Lead Finish:
(A) = Solder
(C) = Gold
(X) = Optional

Screening:
(C) = Mil Temp
(P) = Prototype
(W) = Extended Industrial Temp (-40°C to +125°C)

Package Type:
(U) = 28-lead Flatpack

Access Time:
(45) = 45ns access time, TTL compatible inputs, CMOS/TTL compatible outputs

Device Type Modifier:
(T) = TTL compatible inputs and CMOS/TTL compatible outputs

Device Type:
(28F256QLE) = 32Kx8 One Time Programmable PROM

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an “X” is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
4. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is gold only.
6. Due to the unique nature of field programmed devices, Cobham does not guarantee program yield or accept returns for programming failures. Cobham estimates programming yield at 80% or greater. Users should reference the "QLE Programming Guide" and the "QLE Programming Notes" documents available under the Applications Notes tab of the Cobham HiRel Microelectronics Memory device webpage for programming instructions and information.
Cobham Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development
Preliminary Datasheet - Shipping Prototype
Datasheet - Shipping QML & Reduced Hi-Rel

Revision History:
===========================================================================
March 2007: Initial revision used for change tracking purposes
===========================================================================
Feb 2020: MJL 02/13/2020
1) Added programming yield estimate on page #1
2) Added note 5 to page 8 and note 6 to page 9.
===========================================================================

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