STEP-by-STEP Guide to 1553 Design
Preface

The purpose of this publication is to take a new 1553 designer through the basic steps required to complete a 1553 interface design. The designer will use a system specification and design a hardware implementation (including software routines). The example case begins with a high-level design specification for a black box. Given the 1553 aspects of the system specification the designer will assess the bus traffic verses local memory requirements, select the appropriate protocol device and design the interface. The example black box specification incorporates two of the three 1553 functions (Bus Controller and Remote Terminal).
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1.0 System Specification

1.1 Black Box Overview

The BB (black box) will be designed to accommodate a Bus Controller (BC) and Remote Terminal (RT) function. The BC and RT functions shall operate independently and in a stand-alone fashion. The Bus Controller will transmit the command lists outlined in section 4.2. A status and telemetry table will be maintained within the BC local memory and transmitted from the BB Remote Terminal to the T&C Bus Controller. The status and telemetry assignment and format is outlined in Table 1.

<table>
<thead>
<tr>
<th>Bus Component</th>
<th>S/A#</th>
<th>Telemetry Item</th>
<th>BB Acq Rate</th>
<th>BBRT S/A</th>
<th>T&amp;C Acq Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT #1</td>
<td>3</td>
<td>Critical Sensor 1</td>
<td>200Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Critical Sensor 2</td>
<td>200Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Battery 1 Voltage</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Battery 2 Voltage</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Battery 1 Current</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Battery 2 Current</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td>Bus Component</td>
<td>S/A#</td>
<td>Telemetry Item</td>
<td>BB Acq Rate</td>
<td>BBRT S/A</td>
<td>T&amp;C Acq Rate</td>
</tr>
<tr>
<td>---------------</td>
<td>-----</td>
<td>----------------------</td>
<td>-------------</td>
<td>----------</td>
<td>--------------</td>
</tr>
<tr>
<td>RT #2</td>
<td>3</td>
<td>Critical Sensor 3</td>
<td>200Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Critical Sensor 4</td>
<td>200Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>ACS 1 Voltage</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>ACS 1 Current</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Horizon Sensor 1</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Horizon Sensor 2</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td>RT #3</td>
<td>3</td>
<td>Critical Sensor 5</td>
<td>200Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Critical Sensor 6</td>
<td>200Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Air Pressure AFT</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Air Pressure FRD</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Altimeter 1</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Altimeter 2</td>
<td>100Hz</td>
<td>1</td>
<td>200Hz</td>
</tr>
</tbody>
</table>
Within the system architecture the BB has the responsibility for short loop control function corrections. The BB maintains a table for the purpose of actuator control and feedback, which the T&C requests on a periodic basis. The outer control-loop is controlled by the T&C via a 1553 command sent to the position S/A for each RT. Inner-loop compensation is performed locally by the BB processor. Table 2 outlines the control and position information format.

**Table 2:**

<table>
<thead>
<tr>
<th>Bus Component</th>
<th>S/A#</th>
<th>Actuator Item</th>
<th>BB CMD&amp;Acq Rate</th>
<th>BBRT S/A</th>
<th>T&amp;C Acq Rate</th>
<th>T&amp;C CMD Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT #2</td>
<td>1</td>
<td>Torque #1</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Position #1</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td>100Hz</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Torque #2</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Position #2</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td>100Hz</td>
</tr>
<tr>
<td>RT #3</td>
<td>1</td>
<td>Torque #3</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Position #3</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td>100Hz</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Torque #4</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Position #4</td>
<td>400Hz</td>
<td>1</td>
<td>200Hz</td>
<td>100Hz</td>
</tr>
</tbody>
</table>

The BB sub-system status will be reported back to the T&C through the use of the SSF flag contained in the 1553 status response of the BB Remote Terminal; when the T&C controller receives this status response, a Transmit 1 data word command will be immediately issued to the BB Remote Terminal S/A 2. The BB Remote Terminal will respond with proper Status and the single data word. Refer to Appendix B for the BB Sub-system status word format (S/A 2). A periodic Synchronize Mode Code Command without data will be sent by the T&C Bus Controller, prior to the time-tag roll over; this Mode Code will synchronize the BB and the BB sub-system. All un-mentioned BB S/A’s and MC’s shall be illegalized during initialization.

Based on the above system specification, evaluation regarding the BB architecture and design can be performed. The UT69R000 RISC micro-controller (R000) will be used as the core processor for the BB. Due to the operation of the system, the best telemetry and command solution will probably be the SμMIT-DX; this architecture will allow the R000 to create and maintain a single table in local memory for the maintenance of all telemetry and command items. The use of a protocol device with on-board RAM would be slightly less effective since the processor would have to extract the telemetry and command items from the on-board memory and re-locate them into the processor’s local memory.
2.0 Design Evaluation

Given the system parameters, calculate the 1553 and local memory bus requirements for each 1553 bus interface (RT and BC). For all examples, a 9uS response time will be used.

2.1 BB Remote Terminal

T&C sends a Transmit 26 Data Words Command to S/A #1 every 200Hz (1/5mS).

<table>
<thead>
<tr>
<th>T&amp;C XMIT CMD</th>
<th>20uS</th>
<th>9uS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BB Status Response</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DW 1...DW26</td>
<td>520uS</td>
<td></td>
</tr>
</tbody>
</table>

The duty cycle for the T&C 200Hz command is then expressed in terms of bus transmit time over the command repeat duration.

\[
\frac{569uS}{5 mS} = 11.38\%
\]

Next, consider the T&C command for actuator position.
The T&C sends a Receive 4 Data Words Command to S/A #1 every 100Hz (1/10mS) for actuator position control.

<table>
<thead>
<tr>
<th>T&amp;C RCV CMD</th>
<th>20uS</th>
<th>80uS</th>
<th>9uS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BB Status Response</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DW 1...DW4</td>
<td>20uS</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The duty cycle for the T&C 100Hz command is then expressed in terms of bus transmit time over the command repeat duration. Note the SMMIT bus usage percent is in terms of the 200Hz Frame; even though the 100Hz Frame occurs at half the rate of the 200Hz. This is due to the fact every second time through the 200Hz frame, the additional commands of the 100Hz are combined and sent with the 200Hz Frame commands. Therefore, to quantify a worst case 1553 bus usage vs. local bus, the total of the two should be examined, rather than an average based on the actual occurrence (one 100Hz command frame for every two 200Hz command frames).
Calculation of the total combined bus usage is as follows:

\[
\frac{129\mu S}{10 \text{ mS}} = 1.29\%
\]

Bus Usage = 11.38\% + 1.29\% = 12.67\%

The BB RT local bus time required by the ŠµMMIT versus the 1553 message time is as follows:

\[
\frac{333.36\text{nS} \text{ (Descriptor Read)} + 2.167\mu \text{S} \text{ (Read 26 Data Words)} + 500.04\text{nS} \text{ (Descriptor Update)} + 166.7\text{nS} \text{(Interrupt log)}}{5\text{mS} \text{ (200 Hz cycle time)}} = 0.04\%
\]

\[
\frac{333.36\text{nS} \text{ (Descriptor Read)} + 333.36\text{nS} \text{ (Read 4 Data Words)} + 500.04\text{nS} \text{ (Descriptor Update)} + 166.7\text{nS} \text{(Interrupt log)}}{10\text{mS} \text{ (100 Hz cycle time)}} = 0.09\%
\]

<table>
<thead>
<tr>
<th>ŠµMMIT Bus Usage</th>
<th>4.5\mu S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Cycle Time</td>
<td>5.0\text{mS}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ŠµMMIT Bus Usage</th>
<th>0.09% *</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Cycle Time</td>
<td></td>
</tr>
</tbody>
</table>

*Note:
To minimize the amount of continuous local bus time the ŠµMMIT will require, the ŠµMMIT will be operating in non-buffered mode and have zero wait-states for all memory accesses.

2.2 **BB Bus Controller**

BB sends a Transmit 2 Data Words Command to S/A #3 of RT#1, RT#2 and RT#3 every 200Hz (1/5mS) for Critical Sensor data acquisition.

The duty cycle for the BB 200Hz command is then expressed in terms of bus transmit time over the command repeat duration.

\[
\frac{89uS}{5 mS} = 1.78\% \quad 1.78\% \times 3\text{RT’s} = 5.34\%
\]

BB sends a Transmit 4 Data Words Command to S/A #2 of RT#1, RT#2 and RT#3 every 100Hz (1/10mS) for Housekeeping telemetry items (Battery Voltage, Battery Current, ACS Voltage, Horizon Sensor, Air Pressure and Altimeter).

The duty cycle for the BB 100Hz command is then expressed in terms of bus transmit time over the command repeat duration.

\[
\frac{129uS}{10 mS} = 1.29\% \quad 1.29\% \times 3\text{RT’s} = 3.87\%
\]
BB sends a Transmit 2 Data Words Command to S/A #1 of RT#2 and RT#3 every 400Hz (1/2.5mS) for actuator position acquisition.

\[
\begin{array}{c|c|c}
\text{BB XMIT CMD} & & \\
\hline
\text{RT Status Response} & \text{DW 1} & \text{DW 2} \\
\hline
20uS & 9uS & 20uS & 40uS
\end{array}
\]

The duty cycle for the BB 400Hz command is then expressed in terms of bus transmit time over the command repeat duration.

\[
\frac{89uS}{2.5 \text{ mS}} = 3.56\% \quad 3.56\% \times 2 \text{RT's} = 7.12\%
\]

Finally, consider the BB command for actuator position.
The BB sends a Receive 2 Data Words Command to S/A #1 of RT#2 and RT#3 every 400Hz (1/2.5mS) for actuator position control.

\[
\begin{array}{c|c|c}
\text{BB RCV CMD} & \text{DW 1} & \text{DW 2} \\
\hline
\text{RT Status Response} & & \\
\hline
20uS & 40uS & 9uS
\end{array}
\]

The duty cycle for the BB 400Hz command is then expressed in terms of bus transmit time over the command repeat duration.

\[
\frac{89uS}{2.5 \text{ mS}} = 3.56\% \quad 3.56\% \times 2 \text{RT's} = 7.12\%
\]

Bus Usage  = 7.12\% + 7.12\% + 3.87\% + 5.34\%  
= 23.45\%
The BB BC local bus time required by the SµMMIT versus the 1553 message time is as follows:

\[
[666.72\text{ns (Descriptor Read)} + 166.7\text{ns (Read 2 DW)} + 666.72\text{ns (Descriptor Update)}] \times 3 + 166.7\text{ns (Interrupt log)} \times 3
\]

5mS (200 Hz cycle time)

\[
[666.72\text{ns (Descriptor Read)} + 333.36\text{ns (Read 4 DW)} + 666.72\text{ns (Descriptor Update)}] \times 3 + 166.7\text{ns (Interrupt log)} \times 3
\]

10mS (100 Hz cycle time)

\[
[666.72\text{ (Descriptor Read)} + 166.7\text{ns (Read 2 DW)} + 666.72\text{ (Descriptor Update)}] \times 2 + 166.7\text{ns (Interrupt log)} \times 3
\]

2.5mS (400 Hz cycle time)

\[
[666.72\text{ (Descriptor Read)} + 166.7\text{ns (Read 2 DW)} + 666.72\text{ (Descriptor Update)}] \times 2 + 166.7\text{ns (Interrupt log)} \times 3
\]

2.5mS (400 Hz cycle time)

\[
\text{SµMMIT Bus Usage } = 17.5\mu\text{S}
\]
Frame Cycle Time 2.5mS

\[
\text{SµMMIT Bus Usage } = 0.7%^*
\]
Frame Cycle Time

*Note:
To minimize the amount of continuous local bus time the SµMMIT will require, the SµMMIT will be operating in non-buffered mode and have zero wait-states for all memory accesses.

Bus usage summary:
Accounting for two SµMMIT-DX devices connected to the same local memory bus, (operating in RT and BC mode), with the maximum 1553 Command scenario running simultaneously, the SµMMIT Vs. 1553 Bus time increases to 0.78%. Operating the SµMMIT in the non-buffered mode, distributes more DMA accesses across a broader time range of the overall 1553 message and therefore more local bus accesses. The benefit yielded from this mode of operation is the fact that the Data Word (single word read) DMA access time is greatly reduced. Instead of a (buffered mode) maximum access requirement of 2.167µS (26 Data Words x 41.67nS x2), each SµMMIT demands only 83.33nS for each data word interaction, spaced approximately every 9µS between data word accesses. If both SµMMIT-DX devices align such that each SµMMIT is requesting access at each others respective critical time and the BB processor keeps the bus the maximum amount of time prior to granting access, the longest bus access time would be as follows:
The RT is requesting the longest DMA time of 500.04nS, simultaneously the BC is requesting its maximum DMA time of 666.72nS. Given these conditions, none of the SµMMIT accesses would cause a local bus time-out (7µS RT mode DMA time-out), nor would any processor functions be impeded.

* Note: The R000 processor will grant access to the local memory bus within seven processor clocks (16Mhz x 7 = 438nS).
3.0 Black Box Overview

System Overview
3.2 Data Bus and Control Signals

Now that the basic architecture is established, further definition with respect to the memory mapping of each 1553 protocol device and arbitration logic can be created.

The data bus interface of the R000 is 16 bits wide (D15:D0) and has a (data port) 16 bit address bus (A15:A0). The R000 uses commercially standard types of memory and I/O bus control signals. The control signals are as follows: Memory/Input-Output (M/IO), designates whether the current bus cycle is a Memory (active high), or I/O (Active low) operation; Read/Write (R/WR), designates whether the current bus cycle is a Read (active high), or Write (active low) operation; DS, indicates the current bus cycle data is valid (Write), or the addressed (Read) data should be placed on the data bus; DTACK indicates the current bus cycle active low) can be terminated; BRQ, Bus Request output pin from the R000 requesting control of the local data bus; BGNT, Bus Grant input pin (active low) to the R000, indicates the R000 has been granted control of the local memory bus; BGACK, Bus Grant Acknowledge (active low), indicates the R000 has received the Bus Grant signal and is acknowledging local memory bus access. The SµMMIT-DX data bus interface is very similar to the R000’s. The SµMMIT data and address busses are 16 bits wide (D15:D0) and(A15:A0) respectively. The SµMMIT control signals are as follows:

Chip Select (CS), enables the Host to read or write to the internal SµMMIT registers; Read/Write (R/WR), used in conjunction with CS to perform a SµMMIT register Read (active high), or Write (active low) operation; RWR, indicates the current bus cycle data is valid (Write), RRD, indicates the current bus cycle data the addressed (Read) data should be placed on the data bus; RCS, used in conjunction with RRD or RWR to perform SµMMIT memory accesses; DTACK indicates the current bus cycle (active low) can be terminated; DMAR, DMA Request output pin from the SµMMIT requesting control of the local data bus; DMAG, DMA Grant input pin (active low) to the SµMMIT, indicates the SµMMIT has been granted control of the local memory bus; DMACK, DMA Grant Acknowledge (active low) output pin, indicates the SµMMIT has received and is acknowledging the Bus Grant signal permitting local memory bus access.

3.3 Bus Arbitration

The following describes the arbitration required between both SµMMITs and R000 processor. Since the 1553 is an asynchronous bus and the response is a timed function, the arbiter should provide priority in the following order: 1) 1553 RT, 2) 1553 BC, 3) Local processor.

The arbiter design for this example is contained in Appendix A of this document. The arbitration schematic is provided as a guide and not intended to be used for a final design; issues surrounding timing are application specific and need to be evaluated for each target system. An overview of the arbiter interface is shown below.
### 3.4 Memory and I/O Map

The internal registers of the \( \mu \)MMIT devices will be selected by an I/O operation from the UT69R000. The \( \mu \)MMIT controlling the RT function will have its internal registers mapped starting at location 1000 Hex. The \( \mu \)MMIT controlling the BC function will have its internal registers mapped starting at location 2000 Hex. The I/O address and \( \mu \)MMIT registers correlation is as follows:

<table>
<thead>
<tr>
<th>Register</th>
<th>Physical Address</th>
<th>Function</th>
<th>Physical Address</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>Control</td>
<td>1000</td>
<td>Control</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>Operational Status</td>
<td>1001</td>
<td>Operational Status</td>
</tr>
<tr>
<td>2</td>
<td>0002</td>
<td>Current Command Block</td>
<td>1002</td>
<td>Current Command</td>
</tr>
<tr>
<td>3</td>
<td>0003</td>
<td>Interrupt Mask</td>
<td>1003</td>
<td>Interrupt Mask</td>
</tr>
<tr>
<td>4</td>
<td>0004</td>
<td>Pending Interrupt</td>
<td>1004</td>
<td>Pending Interrupt</td>
</tr>
<tr>
<td>5</td>
<td>0005</td>
<td>Interrupt Log List Pointer</td>
<td>1005</td>
<td>Interrupt Log List Pointer</td>
</tr>
<tr>
<td>6</td>
<td>0006</td>
<td>BIT Word</td>
<td>1006</td>
<td>BIT Word</td>
</tr>
<tr>
<td>7</td>
<td>0007</td>
<td>Minor Frame Timer</td>
<td>1007</td>
<td>Time Tag</td>
</tr>
<tr>
<td>8</td>
<td>0008</td>
<td>Command Block Pointer</td>
<td>1008</td>
<td>SRT Descriptor Pointer</td>
</tr>
<tr>
<td>9</td>
<td>0009</td>
<td>Not Used</td>
<td>1009</td>
<td>1553 Status Word Bits</td>
</tr>
<tr>
<td>10</td>
<td>000A</td>
<td>Cmd Blk initialization count</td>
<td>100A</td>
<td>Not Used</td>
</tr>
<tr>
<td>11</td>
<td>000B</td>
<td>Not Used</td>
<td>100B</td>
<td>Not Used</td>
</tr>
<tr>
<td>12</td>
<td>000C</td>
<td>Not Used</td>
<td>100C</td>
<td>Not Used</td>
</tr>
<tr>
<td>13</td>
<td>000D</td>
<td>Not Used</td>
<td>100D</td>
<td>Not Used</td>
</tr>
<tr>
<td>14</td>
<td>000E</td>
<td>Not Used</td>
<td>100E</td>
<td>Not Used</td>
</tr>
<tr>
<td>15</td>
<td>000F</td>
<td>Not Used</td>
<td>100F</td>
<td>Not Used</td>
</tr>
<tr>
<td>16</td>
<td>0010</td>
<td>Not Used</td>
<td>1010</td>
<td>Receive</td>
</tr>
<tr>
<td>17</td>
<td>0011</td>
<td>Not Used</td>
<td>1011</td>
<td>Receive</td>
</tr>
<tr>
<td>18</td>
<td>0012</td>
<td>Not Used</td>
<td>1012</td>
<td>Transmit</td>
</tr>
<tr>
<td>19</td>
<td>0013</td>
<td>Not Used</td>
<td>1013</td>
<td>Transmit</td>
</tr>
<tr>
<td>20</td>
<td>0014</td>
<td>Not Used</td>
<td>1014</td>
<td>Broadcast Receive</td>
</tr>
<tr>
<td>21</td>
<td>0015</td>
<td>Not Used</td>
<td>1015</td>
<td>Broadcast Receive</td>
</tr>
<tr>
<td>22</td>
<td>0016</td>
<td>Not Used</td>
<td>1016</td>
<td>Broadcast Transmit</td>
</tr>
<tr>
<td>23</td>
<td>0017</td>
<td>Not Used</td>
<td>1017</td>
<td>Broadcast Transmit</td>
</tr>
<tr>
<td>24</td>
<td>0018</td>
<td>Not Used</td>
<td>1018</td>
<td>Mode Code Receive</td>
</tr>
<tr>
<td>25</td>
<td>0019</td>
<td>Not Used</td>
<td>1019</td>
<td>Mode Code Receive</td>
</tr>
<tr>
<td>26</td>
<td>001A</td>
<td>Not Used</td>
<td>101A</td>
<td>Mode Code Transmit</td>
</tr>
<tr>
<td>27</td>
<td>001B</td>
<td>Not Used</td>
<td>101B</td>
<td>Mode Code Transmit</td>
</tr>
<tr>
<td>28</td>
<td>001C</td>
<td>Not Used</td>
<td>101C</td>
<td>Broadcast Mode Code Receive</td>
</tr>
<tr>
<td>29</td>
<td>001D</td>
<td>Not Used</td>
<td>101D</td>
<td>Broadcast Mode Code Receive</td>
</tr>
<tr>
<td>30</td>
<td>001E</td>
<td>Not Used</td>
<td>101E</td>
<td>Broadcast Mode Code Transmit</td>
</tr>
<tr>
<td>31</td>
<td>001F</td>
<td>Not Used</td>
<td>101F</td>
<td>Broadcast Mode Code Transmit</td>
</tr>
</tbody>
</table>

**Diagram:**

- R000
- A15
- A14
- A13
- A12
- M/IO
- DS
- R/WR

- \( \overline{CS1} \) (RT)
- \( \overline{CS2} \) (BC)
- R/WR (RT and BC)
3.5 Housekeeping Table

Each SμMIT will have a region of local memory dedicated for descriptor space. To maximize performance and minimize data manipulation, the Housekeeping Table will be located within a common address range (8000-801D).

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>8000</td>
<td>Torque #1</td>
</tr>
<tr>
<td>8001</td>
<td>Torque #2</td>
</tr>
<tr>
<td>8002</td>
<td>Torque #3</td>
</tr>
<tr>
<td>8003</td>
<td>Torque #4</td>
</tr>
<tr>
<td>8004</td>
<td>Position #1</td>
</tr>
<tr>
<td>8005</td>
<td>Position #2</td>
</tr>
<tr>
<td>8006</td>
<td>Position #3</td>
</tr>
<tr>
<td>8007</td>
<td>Position #4</td>
</tr>
<tr>
<td>8008</td>
<td>Critical Sensor #1</td>
</tr>
<tr>
<td>8009</td>
<td>Critical Sensor #2</td>
</tr>
<tr>
<td>800A</td>
<td>Critical Sensor #3</td>
</tr>
<tr>
<td>800B</td>
<td>Critical Sensor #4</td>
</tr>
<tr>
<td>800C</td>
<td>Critical Sensor #5</td>
</tr>
<tr>
<td>800D</td>
<td>Critical Sensor #6</td>
</tr>
<tr>
<td>800E</td>
<td>Battery #1 Voltage</td>
</tr>
<tr>
<td>800F</td>
<td>Battery #2 Voltage</td>
</tr>
<tr>
<td>8010</td>
<td>Battery #1 Current</td>
</tr>
<tr>
<td>8011</td>
<td>Battery #2 Current</td>
</tr>
<tr>
<td>8012</td>
<td>ACS #1 Voltage</td>
</tr>
<tr>
<td>8013</td>
<td>ACS #1 Current</td>
</tr>
<tr>
<td>8014</td>
<td>Horizon Sensor #1</td>
</tr>
<tr>
<td>8015</td>
<td>Horizon Sensor #2</td>
</tr>
<tr>
<td>8016</td>
<td>Air Pressure AFT</td>
</tr>
<tr>
<td>8017</td>
<td>Air Pressure FRD</td>
</tr>
<tr>
<td>8018</td>
<td>Altimeter #1</td>
</tr>
<tr>
<td>8019</td>
<td>Altimeter #2</td>
</tr>
<tr>
<td>801A</td>
<td>CMD Position #1</td>
</tr>
<tr>
<td>801B</td>
<td>CMD Position #2</td>
</tr>
<tr>
<td>801C</td>
<td>CMD Position #3</td>
</tr>
<tr>
<td>801D</td>
<td>CMD Position #4</td>
</tr>
</tbody>
</table>
4.0 Black Box 1553 Software Initialization

4.1 Black Box configuration setup for the Bus Controller initialization.

Black Box Bus Controller Command Block listing for Minor and Major Frames. Below is an overview of the BC mode command block structure. Each command block requires an allocation of 8 memory locations.

Bus Controller Command Block Format
Address Function
0000 Control Word
0001 Command Word 1
0002 Command Word 2
0003 Data Pointer
0004 Status Word 1
0005 Status Word 2
0006 Branch Address
0007 Timer Value

Command Block Execution:
Once it has been granted access (DMAG=’0’) to the local memory bus, the SµMMIT will read all eight words of the command block from memory in a single burst. The SµMMIT decodes the Command Block control word and performs the instructed operations. Once the appropriate action has been taken, the SµMMIT performs an update of the command block through another DMA burst into memory. If interrupts were enabled and an interrupt condition occurred, there would be a total of eight words (Control Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, Interrupt Status Word and Interrupt Address Word) written into memory during the Command Block update. If interrupts were enabled but no interrupt condition occurred, there would be a total of six words (Control Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1 and Status Word 2) written into memory during the Command Block update. In certain cases, the SµMMIT will not perform a command block update prior to continuing to the next command block; these opcodes (that don’t require the command block update) are listed below.

EOL (end of List), Skip, Go To, Built-in Test, Interrupt and Continue, Call, Return to Call, LMFT (Load Minor Frame Timer) and Return to Branch.

If interrupts are enabled, the op-codes that generate interrupts will cause a two word (Interrupt Status Word and Interrupt Address Word) burst update at the end of message processing.

For further information regarding the SµMMIT Command Block execution refer to the latest Enhanced SµMMIT Family Product Handbook.

4.2 Bus Controller Command Block Listing

For this application, the BC Command blocks will be located at address 2100 Hex (Top of Command Block) and will be initialized by the R000 processor after a system reset. The following list of Command Blocks are the minimum required to perform the required BB Bus Controller function. The Command Block listing could easily be used as a skeleton for a more elaborate Bus Controller command structure, utilizing more of the autonomous SµMMIT features.

After Reset, the R000 writes the following values to the local memory to initialize the BC Command blocks.

BB Major Frame
Executes 3 minor Frames of 100Hz, 200Hz and 400Hz

| [Command Block 1] 400Hz Minor Frame Start |
|-------------------|-------------------|
| [Command Block 1] 400Hz Minor Frame Start |
| Address Data Function |
| 2100 E000 Load Minor Frame Timer |
| 2101 0000 1553 Command 1 (not applicable) |
| 2102 0000 1553 Command 2 (not applicable) |
| 2103 0000 Data address pointer (not applicable) |
Major Frame Timer value = 2.5mS (64uS/bit) for 400Hz. Note: 62.5nS under 2.5mS.

[Command Block 2] Sample Actuator positions 1 and 2

Address Data Function
2108  4200 Execute and continue
2109  1422  1553 Command: RT#2, Transmit, SA#1, Data words = 2, Bus=A
210A  0000  1553 Command 2 (not applicable)
210B  8004  Data address pointer (Housekeeping Table)
210C  0000  Status Word 1
210D  0000  Status Word 2
210E  0000  Branch address
210F  0000  Timer value

[Command Block 3] Sample Actuator positions 3 and 4

Address Data Function
2110  4200 Execute and continue
2111  1C22  1553 Command: RT#3, Transmit, SA#1, Data words = 2, Bus=A
2112  0000  1553 Command 2 (not applicable)
2113  8006  Data address pointer (Housekeeping Table)
2114  0000  Status Word 1
2115  0000  Status Word 2
2116  0000  Branch address
2117  0000  Timer value

[Command Block 4] Send Torque Commands 1 and 2

Address Data Function
2118  4200 Execute and continue
2119  1022  1553 Command: RT#2, Receive, SA#1, Data words = 2, Bus=A
211A  0000  1553 Command 2 (not applicable)
211B  8000  Data address pointer (Housekeeping Table)
211C  0000  Status Word 1
211D  0000  Status Word 2
211E  0000  Branch address
211F  0000  Timer value
[Command Block 5] Send Torque Commands 3 and 4
Address Data Function
2120 4200 Execute and continue
2121 1822 1553 Command: RT#3, Receive, SA#1, Data words = 2, Bus=A
2122 0000 1553 Command 2 (not applicable)
2123 8002 Data address pointer (Housekeeping Table)
2124 0000 Status Word 1
2125 0000 Status Word 2
2126 0000 Branch address
2127 0000 Timer value

[Command Block 6] Send Interrupt to the R000 to alert the completion of the 400Hz Minor Frame
Address Data Function
2128 A000 Interrupt and continue
2129 0000 1553 Command 1 (not applicable)
212A 0000 1553 Command 2 (not applicable)
212B 0000 Data address pointer (not applicable)
212C 0000 Status Word 1
212D 0000 Status Word 2
212E 0000 Branch address
212F 0000 Timer value

[Command Block 7] Frame selection occurs here (Back to top of 400Hz MF, or continue to 200Hz MF)
Address Data Function
2130 2000 GOTO
2131 0000 1553 Command 1 (not applicable)
2132 0000 1553 Command 2 (not applicable)
2133 0000 Data address pointer (not applicable)
2134 0000 Status Word 1
2135 0000 Status Word 2
2136 2100 Branch address - The first time through, send the µMMIT back to the beginning of the 400Hz MF
2137 0000 Timer value

200Hz Minor Frame Start
[Command Block 1] Sample Critical Sensors 1 and 2
Address Data Function
2138 4200 Execute and continue
2139 0C62 1553 Command: RT#1, Transmit, SA#3, Data words = 2, Bus=A
213A 0000 1553 Command 2 (not applicable)
213B 8008 Data address pointer (Housekeeping Table)
213C 0000 Status Word 1
213D 0000 Status Word 2
213E 0000 Branch address
213F 0000 Timer value

[Command Block 2] Sample Critical Sensors 3 and 4
Address Data Function
2140 4200 Execute and continue
2141 1462 1553 Command: RT#2, Transmit, SA#3, Data words = 2, Bus=A
2142 0000 1553 Command 2 (not applicable)
2143 800A Data address pointer (Housekeeping Table)
2144 0000 Status Word 1
2145 0000 Status Word 2
2146 0000 Branch address
2147 0000 Timer value
[Command Block 3] Sample Critical Sensors 5 and 6
Address Data Function
2148 4200 Execute and continue
2149 1C62 1553 Command: RT#3, Transmit, SA#3, Data words = 2, Bus=A
214A 0000 1553 Command 2 (not applicable)
214B 800C Data address pointer (Housekeeping Table)
214C 0000 Status Word 1
214D 0000 Status Word 2
214E 0000 Branch address
214F 0000 Timer value

[Command Block 4] Send Interrupt to the R000 to alert the completion of the 200Hz Minor Frame
Address Data Function
2150 A000 Interrupt and continue
2151 0000 1553 Command 1 (not applicable)
2152 0000 1553 Command 2 (not applicable)
2153 0000 Data address pointer (not applicable)
2154 0000 Status Word 1
2155 0000 Status Word 2
2156 0000 Branch address
2157 0000 Timer value

[Command Block 5] Frame selection occurs here (Back to top of 400Hz MF, or continue to 100Hz MF).
Address Data Function
2158 2000 GOTO
2159 0000 1553 Command 1 (not applicable)
215A 0000 1553 Command 2 (not applicable)
215B 0000 Data address pointer (not applicable)
215C 0000 Status Word 1
215D 0000 Status Word 2
215E 2100 Branch address - The first time through, send the $\mu$MMIT back to the beginning of the 400Hz MF
215F 0000 Timer value

100Hz Minor Frame Start
[Command Block 1] Sample Battery 1-2 Voltage and Current
Address Data Function
2160 4200 Execute and continue
2161 0C44 1553 Command: RT#1, Transmit, SA#2, Data words = 4, Bus=A
2162 0000 1553 Command 2 (not applicable)
2163 800E Data address pointer (Housekeeping Table)
2164 0000 Status Word 1
2165 0000 Status Word 2
2166 0000 Branch address
2167 0000 Timer value

[Command Block 2] Sample ACS and Horizon sensors
Address Data Function
2168 4200 Execute and continue
2169 1444 1553 Command: RT#2, Transmit, SA#2, Data words = 4, Bus=A
216A 0000 1553 Command 2 (not applicable)
216B 8012 Data address pointer (Housekeeping Table)
216C 0000 Status Word 1
216D 0000 Status Word 2
216E 0000 Branch address
216F 0000 Timer value
[Command Block 3] Sample Air Pressure and Altimeter sensors
Address Data Function
2170 4200 Execute and continue
2171 1C44 1553 Command: RT#3, Transmit, SA#2, Data words = 4, Bus=A
2172 0000 1553 Command 2 (not applicable)
2173 8016 Data address pointer (Housekeeping Table)
2174 0000 Status Word 1
2175 0000 Status Word 2
2176 0000 Branch address
2177 0000 Timer value

[Command Block 4] Send Interrupt to the R000 to alert the completion of the 100Hz Minor Frame
Address Data Function
2178 A000 Interrupt and continue
2179 0000 1553 Command 1 (not applicable)
217A 0000 1553 Command 2 (not applicable)
217B 0000 Data address pointer (not applicable)
217C 0000 Status Word 1
217D 0000 Status Word 2
217E 0000 Branch address
217F 0000 Timer value

[Command Block 5] Always return to top of 400Hz MF.
Address Data Function
2180 2000 GOTO
2181 0000 1553 Command 1 (not applicable)
2182 0000 1553 Command 2 (not applicable)
2183 0000 Data address pointer (not applicable)
2184 0000 Status Word 1
2185 0000 Status Word 2
2186 2100 Branch address - Send the ŠuMMIT back to the beginning of the 400Hz MF
2187 0000 Timer value

4.3 Bus Controller Register Setup.

After Reset, the R000 writes the following values to the internal registers of the ŠuMMIT to initialize and begin the BC mode of operation.

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000</td>
<td>2003 0002</td>
<td>Interrupt Mask = [Enable CBA Interrupt]</td>
</tr>
<tr>
<td>R000 write &gt;</td>
<td>2005 2200</td>
<td>Interrupt Log List Pointer= Address 2200 Hex</td>
</tr>
<tr>
<td>R000 write &gt;</td>
<td>2008 2100</td>
<td>Command Block Pointer = [400Hz Command Block 1]</td>
</tr>
<tr>
<td>R000 write &gt;</td>
<td>2000 8002</td>
<td>Control Register = [Start Execution, Enable Interrupt Logging]</td>
</tr>
</tbody>
</table>

As the ŠuMMIT executes the Command Blocks, the R000 waits for the MSG_INT to occur. The interrupt serves two purposes; to synchronize the R000 with the 1553 command blocks and to alert the R000 as to where within the Major Frame the Bus Controller is currently executing. The R000 modifies the jump location to select the appropriate Minor Frame execution path. The following diagram illustrates the Minor Frame execution path and the R000 interaction based upon the interrupts.
4.4 **Bus Controller Command Execution Flow Chart.**

- **Start 400Hz Command Block**
- **Load Minor Frame Timer**
  - **Previous Count=0?**
    - Yes: **Execute 400Hz CMDs**
    - No: Wait until MFT counts to zero
  - **Interrupt>R000**
  - **GOTO 2100**
  - **GOTO 2138**
  - **GOTO 2100**
  - **GOTO 2138**

  **R000 Interaction**
  - 1st loop: Top of 400Hz Command Block Address
  - 2nd loop: Top of 200Hz Command Block Address
  - 3rd loop: Top of 400Hz Command Block Address
  - 4th loop: Top of 200Hz/100Hz Command Block Addresses

- **Start 200Hz Command Block**
  - Execute 200Hz CMDs
  - Send Interrupt>R000
  - **GOTO 2100**
  - **GOTO 2160**

- **Start 100Hz Command Block**
  - Execute 100Hz CMDs
  - Send Interrupt>R000
  - **GOTO 2100**
4.5 Remote Terminal Descriptor Format.

Below is an overview of the RT mode Descriptor block structure. Each S/A requires an allocation of 4 memory locations for the associated RT descriptor. The RT descriptor space will be located in local memory starting at address 1100 Hex.

Remote Terminal and Mode Code Descriptor Format (Using Mode 2)

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Control Word</td>
</tr>
<tr>
<td>0001</td>
<td>Top Address</td>
</tr>
<tr>
<td>0002</td>
<td>Current Address</td>
</tr>
<tr>
<td>0003</td>
<td>Message Information Buffer Address</td>
</tr>
</tbody>
</table>

The Remote Terminal Descriptor execution is as follows:
Once it has been granted access (DMAG = “0”) to the local memory bus, the SmMIT will read all four words of the descriptor block from memory in a single burst. The SmMIT decodes the Control word and reacts to the received 1553 message based on the Descriptor information. Once the 1553 message is complete, the SmMIT performs an update of the Descriptor block and Message Information Buffer through another DMA burst into memory. If interrupts were enabled and an interrupt condition occurred, there would be a total of six words (Message Information Word, Time Tag, Current Address, Control Word, Interrupt Information Word and Interrupt Address Word) written into memory during the Descriptor Block and MIB update. If interrupts were enabled but no interrupt condition occurred, there would be a total of four words (Message Information Word, Time Tag, Current Address, Control Word) written into memory during the Descriptor Block and MIB update. For further information regarding the SmMIT Descriptor Block and Message Information Buffer, refer to the latest Enhanced SmMIT Family Product Handbook.

4.6 Remote Terminal Descriptor Listing

For this application, the RT Descriptor blocks will be located at address 1100 Hex (Top of Descriptor Space) and will be initialized by the R000 processor after a system reset.
After Reset, the R000 writes the following values to the local memory to initialize the RT Descriptor space. The only S/A’s and Mode Codes that are initialized are the ones used; all others (not used) are illegalized and therefore will be initialized to all zeros.

Descriptor Block Initialization

[S/A1 1553 Receive Command]

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1104</td>
<td>0140</td>
<td>Control Word Set buffer to wrap after one message, set IWA bit to true.</td>
</tr>
<tr>
<td>1105</td>
<td>801A</td>
<td>Top Address Point to the 1st (top) Torque Command</td>
</tr>
<tr>
<td>1106</td>
<td>801A</td>
<td>Current Address</td>
</tr>
<tr>
<td>1107</td>
<td>0000</td>
<td>Message Information Buffer Address</td>
</tr>
</tbody>
</table>

[S/A1 1553 Transmit Command]

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1184</td>
<td>0140</td>
<td>Control Word Set buffer to wrap after one message, set IWA bit to true.</td>
</tr>
<tr>
<td>1185</td>
<td>8000</td>
<td>Top Address Point to the Top of the Housekeeping Table</td>
</tr>
<tr>
<td>1186</td>
<td>8000</td>
<td>Current Address</td>
</tr>
<tr>
<td>1187</td>
<td>0004</td>
<td>Message Information Buffer Address</td>
</tr>
</tbody>
</table>

[S/A2 1553 Transmit Command]

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1188</td>
<td>0140</td>
<td>Control Word Set buffer to wrap after one message, set IWA bit to true.</td>
</tr>
<tr>
<td>1189</td>
<td>F777</td>
<td>Top Address Point to the system status word</td>
</tr>
<tr>
<td>118A</td>
<td>F777</td>
<td>Current Address</td>
</tr>
<tr>
<td>118B</td>
<td>0008</td>
<td>Message Information Buffer Address</td>
</tr>
</tbody>
</table>
4.7 Remote Terminal Register Setup

After Reset, the R000 writes the following values to the internal registers of the SuMMIT to initialize and begin the RT mode of operation.

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1003</td>
<td>0400</td>
<td>Interrupt Mask = [Enable S/A accessed Interrupt]</td>
</tr>
<tr>
<td>1005</td>
<td>1400</td>
<td>Interrupt Log List Pointer = Address 1400 Hex</td>
</tr>
<tr>
<td>1008</td>
<td>1100</td>
<td>Remote Terminal Descriptor Block Pointer = [S/A0 1553 Receive Command]</td>
</tr>
<tr>
<td>1010</td>
<td>FF7D</td>
<td>Illegalization Register = [Receive S/A 1 Legal, 0, 2-15 Illegal]</td>
</tr>
<tr>
<td>1011</td>
<td>FFFF</td>
<td>Illegalization Register = [Receive S/A 16-31 Illegal]</td>
</tr>
<tr>
<td>1012</td>
<td>FFFF9</td>
<td>Illegalization Register = [Transmit S/A 1 and 2 Legal, 0, 3-15 Illegal]</td>
</tr>
<tr>
<td>1013</td>
<td>FFFF</td>
<td>Illegalization Register = [Transmit S/A 16-31 Illegal]</td>
</tr>
<tr>
<td>1014</td>
<td>FFFF</td>
<td>Illegalization Register = [Receive Broadcast S/A 0-15 Illegal]</td>
</tr>
<tr>
<td>1015</td>
<td>FFFF</td>
<td>Illegalization Register = [Receive Broadcast S/A 16-31 Illegal]</td>
</tr>
<tr>
<td>1018</td>
<td>FFFF</td>
<td>Illegalization Register = [Receive Mode Code S/A 1 Legal, 0 and 2-15 Illegal]</td>
</tr>
<tr>
<td>1019</td>
<td>FFFF</td>
<td>Illegalization Register = [Receive Mode Code S/A 16-31 Illegal]</td>
</tr>
<tr>
<td>101A</td>
<td>FFFF</td>
<td>Illegalization Register = [Transmit Mode Code S/A 0-15 Illegal]</td>
</tr>
<tr>
<td>101B</td>
<td>FFFF</td>
<td>Illegalization Register = [Transmit Mode Code S/A 16-31 Illegal]</td>
</tr>
<tr>
<td>101C</td>
<td>FFFF</td>
<td>Illegalization Register = [Broadcast Receive Mode Code S/A 0-15 Illegal]</td>
</tr>
<tr>
<td>101D</td>
<td>FFFF</td>
<td>Illegalization Register = [Broadcast Receive Mode Code S/A 16-31 Illegal]</td>
</tr>
<tr>
<td>101E</td>
<td>FFFF</td>
<td>Illegalization Register = [Broadcast Transmit Mode Code S/A 0-15+ Illegal]</td>
</tr>
<tr>
<td>1000</td>
<td>9982</td>
<td>Control Register = [Start Execution, Enable Interrupt Logging, CH A&amp;B enabled]</td>
</tr>
</tbody>
</table>

* Note: SuMMIT will be operating in 1553B mode only, therefore the Broadcast Transmit Mode Code S/A 16-31 are internally illegalized by the SuMMIT.

The SuMMIT responds to the incoming 1553 commands and since the interrupt when accessed bit is set for legal S/A and Mode Codes, alerting the R000 to each message transfer.
5.0 1553 Bus Interface

The board layout should place the SuMMIT-DX close to the 1553 transformer, locate the transformer close to the 1553 bus connector and eliminate ground and power planes from beneath the transformer. An example layout is illustrated below.
Appendix A

VHDL description for priority encoder

package PRIORITY is
   -- declare a 3 x 8 Array called ORDER
   constant ORDER_WIDTH: INTEGER:= 3;
   subtype ORDER_WORD is BIT_VECTOR (1 to ORDER_WIDTH);
   subtype ORDER_RANGE is INTEGER range 0 to 7;
   type ORDER_TABLE is array (0 to 7) of ORDER_WORD;
   constant ORDER: ORDER_TABLE:= ORDER_TABLE'(
      "000", -- 000
      "001", -- 001
      "010", -- 010
      "001", -- 011
      "100", -- 100
      "001", -- 101
      "010", -- 110
      "001"); -- 111
end PRIORITY;

use PRIORITY.all;

entity priorenc is
   port(addr: in ORDER_RANGE;
       data: out ORDER_WORD);
end;

architecture behavior of priorenc is
   begin
      data <= ORDER(addr);
   end behavior;
Appendix B

BB Remote Terminal S/A 2 data word format

Bit 0: RT#1 SSF (Sub-System Fail)
Bit 1: RT#1 SRQ (Service Request)
Bit 2: RT#1 INS (Instrumentation)
Bit 3: RT#1 TF (Terminal Flag)

Bit 4: RT#2 SSF (Sub-System Fail)
Bit 5: RT#2 SRQ (Service Request)
Bit 6: RT#2 INS (Instrumentation)
Bit 7: RT#2 TF (Terminal Flag)

Bit 8: RT#3 SSF (Sub-System Fail)
Bit 9: RT#3 SRQ (Service Request)
Bit A: RT#3 INS (Instrumentation)
Bit B: RT#3 TF (Terminal Flag)