Table 1: Cross Reference of Applicable Products

<table>
<thead>
<tr>
<th>PRODUCT NAME</th>
<th>MANUFACTURER PART NUMBER</th>
<th>SMD #</th>
<th>DEVICE TYPE</th>
<th>INTERNAL PIC NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>RadTol Eclipse FPGA</td>
<td>UT6325</td>
<td>5962-04229</td>
<td>Non-volatile FPGA</td>
<td>WF01G</td>
</tr>
</tbody>
</table>

1.0 **Overview**

Cobham designed the UT6325 FPGA using antifuse (ViaLink) technology licensed from QuickLogic Corporation. The UT6325 is a one-time programmable, non-volatile FPGA. The UT6325 is a derivative product from the QuickLogic Eclipse QL6325. Cobham used “RadHard-by-Design” techniques to improve SEE and TID performance for the UT6325. Radiation test results are included in the FAQs. Design tools for the UT6325 include industry standard tools for synthesis and simulation and QuickLogic provided tools for place & route and programming. Design tools are included in the FAQs. Current UT6325 package offerings are ceramic only. Package discussions are also included in the FAQs.
2.0 **Frequently Asked Questions (FAQs)**

1) What kind of products will Cobham provide using the QuickLogic ViaLink technology?
   a. Cobham offers the UT6325 non-volatile, 0.25um RadTol Eclipse FPGA based on the QuickLogic ViaLink technology. The UT6325 was radiation hardened using Cobham “RadHard-by-Design” techniques to provide a 70,000 logic gate, 55,300 SRAM bit FPGA suitable for all space applications.

2) What is the procurement vehicle for this product? Are DLA SMD numbers assigned?
   a. Procurement vehicles are the data sheet for prototype and HiRel product (UT*** part numbers) and the SMD for QML production (SMD part #5962-04229). The device is available as a QML-Q, -Q+ or -V device and either 100krad or 300krad TID tolerance.

3) What are the package options for the UT6325?
   a. Packages for the UT6325 include ceramic quad flatpacks (CQFP) and ceramic land or column grid arrays (CLGA, CCGA). Please contact the factory for plastic package requests. The following table references the ceramic package options:

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Description</th>
<th>40 - - YY Detail Drawing</th>
<th>44xxx Outline Drawing</th>
<th>45- Bond Diagram</th>
<th>I/O Count</th>
<th>Clock High Drive Input Count</th>
<th>Vcc, Vccio Count</th>
<th>Ground Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>208W</td>
<td>208 CQFP</td>
<td>74053</td>
<td>44184</td>
<td>45-0663-00</td>
<td>99</td>
<td>9, 16</td>
<td>18, 16</td>
<td>21</td>
</tr>
<tr>
<td>288W</td>
<td>288 CQFP</td>
<td>74072</td>
<td>44219</td>
<td>45-0742-00</td>
<td>163</td>
<td>9, 16</td>
<td>26, 16</td>
<td>29</td>
</tr>
<tr>
<td>484M</td>
<td>484 CLGA, no caps</td>
<td>72006</td>
<td>44220</td>
<td>45-0748-00</td>
<td>316</td>
<td>9, 16</td>
<td>34, 24</td>
<td>45</td>
</tr>
<tr>
<td>484N</td>
<td>484 CCGA, no caps</td>
<td>72006</td>
<td>44221</td>
<td>45-0748-00</td>
<td>316</td>
<td>9, 16</td>
<td>34, 24</td>
<td>45</td>
</tr>
<tr>
<td>484M</td>
<td>484 CLGA, with caps</td>
<td>72006</td>
<td>44230</td>
<td>45-0748-00</td>
<td>316</td>
<td>9, 16</td>
<td>34, 24</td>
<td>45</td>
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<td>45-0748-00</td>
<td>316</td>
<td>9, 16</td>
<td>34, 24</td>
<td>45</td>
</tr>
</tbody>
</table>
4) Does Cobham provide lead forming guidelines for the CQFP packages?
   a. Yes. Please reference the Cobham web site for the RadTol Eclipse FPGA. Links at this website provide access to lead forming guidelines for the 208CQFP and 288CQFP.
      

5) What are the radiation goals for the UT6325?
   a. 

      Radiation Goals for Cobham RadTol Eclipse
      
      | Radiation Goals                          | Value                      |
      |------------------------------------------|-----------------------------|
      | Total Ionizing Dose                      | 100 / 300 krad(Si)          |
      | Single Event Latchup (SEL)               | >120MeV·cm²/mg at 125°C     |
      | Single Event Upset (SEU)                 | <10 E-8 errors/bit-day      |

   b. Please contact the Cobham factory for a detailed radiation report summarizing SEE testing and results.

6) What orbits does the RadTol Eclipse support?
   a. LEO, MEO, HEO, GEO (low, medium, high and geosynchronous earth orbits), deep space and all other space missions.

7) What is the reliability FIT rate for the UT6325?
   a. The TSMC 0.25um process with the QuickLogic ViaLink technology supports <10 FITs. Cobham is compiling the results of HTOL / LTOL analysis on the UT6325 to support a device rate of <10FITs.

   b. Please contact the Cobham factory for a detailed report summarizing reliability testing and results.
8) What voltage supplies are required for the UT6325?
   a. The UT6325 is a dual voltage device. It has a core voltage supply (Vcc) which is nominally 2.5V (2.3V – 2.7V operating range) and an I/O voltage supply (Vccio) which is nominally 3.3V (3.0V – 3.6V operating range). The I/O buffers are broken into 8 separate banks, so there are 8 individual Vccios, each of which requires its’ own 3.3V supply.

9) Since the Vcc and Vccio are different power supplies (Vcc=2.5V, Vccio=3.3V), is there a required sequence to providing power to the device?
   a. There are no functional failures on the UT6325 regardless of power sequence. There are also no in-rush current effects regardless of power sequencing. The highest Vccio current observed sequencing = 280mA. Cobham results from power sequence testing (see oscilloscope images below):
      i. Vcc and Vccio ramped simultaneously, minor noise of <250mV seen on I/O until Vcc > 1.2V
      ii. Vcc is powered up prior to Vccio, no noise seen on I/O
      iii. When Vccio is powered up prior to Vcc, major noise pulse occurs on I/O pad
          1. Pulse occurs as Vccio increases from ~.8V to ~1.8V
          2. I/O pad voltage appears to follow Vccio
          3. I/O pad appears to tristate when Vccio reaches mid-band (~1.6V)
          4. I/O pad drives High to Vccio at Vcc > 0.8V
          5. I/O resets low with Vcc > 1.2V
          6. Pulse occurs prior to device reaching stable operating voltages
   b. Cobham recommendations
      i. 1) If possible, Ramp Vcc supply prior Vccio
      ii. 2) If necessary, ramp supplies as close to simultaneous as reasonable
      iii. 3) Minimize time when supplies are at mid-range
      iv. 4) Minimize power supply noise and overshoot
      v. 5) Vcc offset ≤ 300mV (i.e. Vcc start at power-up) to fully activate POR
10) Can the UT6325 RadTol Eclipse run with a negative voltage supply, i.e., with Vcc connected to ground and Vss connected to -2.5V?

   a. Yes, since you maintain the same 2.5V potential difference between Vcc power and Vss ground. Please remember that all data inputs must now respect this new voltage bias.

11) Are the UT6325 I/O buffers 5V tolerant?

   a. No. Cobham designed the ESD protection networks to accept 5V inputs, so long as the current is limited. However, the UT6325 cannot meet 5V specifications for Voh and Vol (i.e. cannot drive 5V out). Cobham has an application note for interfacing the UT6325 FPGA to 5V devices located at:

12) What are the I/O buffer capabilities on the UT6325?
   a. There are 8 separate I/O banks on the UT6325. Each I/O bank has a separate Vccio. The UT6325 accepts either 2.5V or 3.3V for Vccio. Cobham qualified the UT6325 using only 3.3V for the Vccio. So, for space applications, the Vccio should be 3.3V. The 3.3V I/O may interface to PCI, LVTTL or LVCMOS buffers. Cobham did not qualify the I/O at the differential voltages for GTL+, SSTL2 or SSTL3. However, with the addition of an external resistor or resistor divider network, the 3.3V I/O may interface to LVDS and LVPECL buffers. The I/O buffer cell contains registers for storing the DataIn, DataOut or OutEnable signals internally. The I/O buffer cell also contains a pull-down resistor. The QuickWorks Constraint Manager can activate the pull-down during place and route activities.

13) How many SRAM cells are available on the UT6325? How can they be configured? Do they require EDAC?
   a. The UT6325 contains 24 dual-port SRAM cells, each with two read (synchronous, asynchronous) and one write (synchronous) port. Each SRAM block contains 2304 bits and can be configured as 128x18, 256x9, 512x4 or 1024x2. The SRAM cells were hardened by Cobham using RadHard-by-Design techniques, so no EDAC is required. The QuickWorks / SpDE tools contain a Wizard that will configure the SRAM blocks into RAM or FIFO implementations. The Wizard will combine SRAM blocks to create a larger address depth or wider word width. The Wizard outputs a VHDL or Verilog netlist that allows the user to instantiate the RAM or FIFO macro into their design.

14) What is the worst case skew for a global or dedicated clock distribution network, given worst case military conditions.
   a. Worst case skew will not exceed 550ps for dedicated or global clock resources.

15) Are there a maximum number of loads for a dedicated or global clock network?
   a. No. The dedicated clock and each global clock contain a distribution network that is sufficiently buffered to be able to drive all register loads within the UT6325 FPGA.

16) Is the interface of the QuickLogic commercial QL6325 FPGA identical to the Cobham UT6325 RadTol Eclipse FPGA in terms of driver capability.
   a. Yes, the I/O interface and the drive capability is the same for both the QL6325 and the UT6325. All of the bidirectional I/O are 3.3V LVCMOS3 compliant. The clocks and high drive I/O (dedicated clock, global clocks, quadrant clocks, IOCNTRL high drive inputs) are 2.5V I/O that are LVCMOS3 compliant.
17) How do you terminate unused I/Os?
   a. The QuickWorks / SpDE software ties off all unused bidirectional I/O internally. The user selects if the tie-off is to Vccio, GND or tri-state. Tie-offs to Vccio or GND use a tie-off structure consisting of a 200 ohm resistor in series with an N-channel transistor. ViaLinks assigned during programming control the gate to the transistor. When activated, the tie-off structures have a nominal current of ~75uA with a Vccio=3.3V. Input only (i.e. clocks and high drive inputs) and special purpose pins should be terminated at the board level. CLKs (dedicated, global, quadrant), IOCTRL and INREF pins should be tied to GND. If the PLLs are not used, the Vccpl, PLLRST and PLLOUT should all be tied to GND. If JTAG is not used, the TRSTB should be connected to GND (to activate the JTAG reset) and the TDI, TMS and TCK should all be connected to Vcc. The JTAG TDO should be left unconnected.

18) Are there absolute maximum input rise and/or fall times?
   a. The Cobham specifications do not state a maximum rise or fall time for input signals to guarantee the stated propagation delay times in the datasheet. Tprop delays are unaffected by input rise and fall times when the rise/fall times are within a reasonable range of 5ns to 20ns and the inputs are monotonic and well behaved. When input rise times are fast (<5ns), overshoot, ringing and reflections may occur which affect the Tprop. Similarly, when input rise/fall times are slow (>20ns), one may experience long signal delays caused by the slow input signal reaching and slowly traversing the input switch point. Long times traversing the switch point, and signals traversing back and forth through the switch point create long Tprop delays.

19) How can you use a falling clock edge?
   a. Flip-flops in the Cobham UT6325 are positive edge triggered. The Dedicated clock connects directly to these flip-flops, so it cannot trigger falling edge devices. For falling edge clocks, the user should invert the clocking signal then place it back on a global or quadrant clock to connect to the falling edge triggered flip-flops. For example, ckpad_25um -> inverter -> gclkbuff_25um or inpad_25um -> inverter -> gclkbuff_25um.

20) How do I assign a High Drive I/O Control network?
   a. To use the IOCONTROL high drive inputs, the user must instantiate the high drive pad into their RTL design. Instantiate the hdpad_25um primitive, then place it using the Constraint Manager in QuickWorks.
21) Which design tools support the Cobham UT6325? What is the normal design flow?

a. The Cobham UT6325 follows a standard FPGA design flow: behavioral simulation, synthesis, place & route, timing analysis and gate level simulation. Cobham provides QuickWorks / SpDE for the place & route, timing analysis and fuse map generation (design_name.lof). Cobham also provides the fuse programming tool, QuickPro for programming UT6325 FPGAs on System General T9600-A programmers. Industry standard tools from Mentor, Aldec and Synopsys provide simulation and synthesis. For simulation, the QuickWorks installation contains primitive and macro libraries for gate level simulation (/pasic/spde/data/...). For synthesis, the user targets the QL6325 FPGA in the QuickLogic Eclipse family. The QuickWorks tools retarget the design netlist to the UT6325 during place & route.

b. For recent design tools supporting this flow, see table below.

<table>
<thead>
<tr>
<th>Function</th>
<th>Tool</th>
<th>Revision</th>
<th>Description</th>
<th>Operating System</th>
<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Place &amp; Route, STA</td>
<td>QuickWorks / SpDE</td>
<td>2010.4.1</td>
<td>Contains patch for installing Cobham timing libraries and package types.</td>
<td>Windows XP. Windows 7</td>
<td>Cobham</td>
</tr>
<tr>
<td>Programming</td>
<td>QuickPro</td>
<td>1.32G</td>
<td>Contains Cobham HiRel programming algorithm</td>
<td>Windows XP.</td>
<td>Cobham</td>
</tr>
<tr>
<td>Synthesis</td>
<td>Synplify Pro</td>
<td>G-2012.09</td>
<td>Last revision to include QuickLogic Eclipse Family</td>
<td>no issue</td>
<td>Synopsys</td>
</tr>
<tr>
<td></td>
<td>Precision Synthesis</td>
<td>2016.1.1</td>
<td>Current revision includes QuickLogic Eclipse Family</td>
<td>no issue</td>
<td>Mentor</td>
</tr>
<tr>
<td>Simulation</td>
<td>Active-HDL / Riviera Pro</td>
<td>current version</td>
<td>Requires Cobham primitive / timing libraries</td>
<td>no issue</td>
<td>Aldec</td>
</tr>
<tr>
<td></td>
<td>ModelSim / QuestaSim</td>
<td>current version</td>
<td>Requires Cobham primitive / timing libraries</td>
<td>no issue</td>
<td>Mentor</td>
</tr>
</tbody>
</table>
22) What is the pricing for parts and design tools?
   a. For pricing on prototype, HiRel and QML production parts, Please contact your Cobham Regional Sales Manager or Product Marketing Manager.
   b. The QuickWorks / SpDE and QuickPro installs are available free of charge. Please contact your Cobham Regional Sales Manager or Product Marketing Manager.
   c. Cobham recommends contacting Mentor, Aldec and Synopsys directly to obtain pricing and support for their tools.

23) What IP is available to the customer?
   a. Cobham recommends Cobham Gaisler for soft IP. Other 3rd party vendors such as Synopsys, Mentor and OpenCores provide Verilog / VHDL netlists and test benches for use with the Cobham UT6325.

24) What was “Lessons Learned” from recent design activity?
   a. The “pull_ff_into_io” command does not work in QuickWorks / SpDE 2010.4.1. This command is normally implemented with the Constraint Manager or editing the .qcf constraint file. Neither of these methods works in 2010.4.1.
   b. The default slew rate defined in the Constraint Manager, Configuration Editor is “DEFAULT (FAST)”. In fact, the default slew rate is SLOW. Cobham confirmed this by verifying .lof files and physical layouts.
   c. QuickWorks / SpDE 2010.4.1 is a Windows XP based tool. It runs on Windows 7 using the Microsoft compatibility application. QuickPro is a Windows XP based tool. This tool does not run in Windows 7 due to hardware driver requirements.
   d. Design FIFO / RAM requirements rapidly deplete the flip-flop resources available on the UT6325. The 1526 cells provide 3052 RadTol registers. Since the logic cell on the UT6325 contains blocks of combinatorial logic with the registers, memory requirements can also waste blocks of logic. To make use of UT6325 resources, it is important to use the 24 SRAM blocks (55,300 bits) for internal RadTol storage. The SRAM blocks have the best SEE performance of the storage elements and greatly reduce the design demands on registers and logic cells. The state machines, logic and muxing portion of the design can now be placed in the logic cell fragments.
   e. Synthesis tools must target the QuickLogic QL6325 device from the Eclipse family. QuickWorks retargets the design to the Cobham UT6325 when the .qdf netlist is imported. Reference the tool table above for synthesis versions supporting the QuickLogic Eclipse.
3.0 **Summary and Conclusion**

For more information about our UT6325 RadTol Eclipse FPGA and other products, please visit our website, [www.cobham.com/HiRel/](http://www.cobham.com/HiRel/).

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**REVISION HISTORY**

<table>
<thead>
<tr>
<th>Date</th>
<th>Rev. #</th>
<th>Author</th>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11/12/2017</td>
<td>1.0.0</td>
<td>RBL</td>
<td>Re-edit and release.</td>
</tr>
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