Standard Product
Cold Sparing Operation and Implementation for the
UT65CML8X8FD 3.125 Gbps Crosspoint Switch (XPS)
Application Note
Cobham.com/HiRel
January 14, 2019

The most important thing we build is trust

Table 1: Cross Reference of Applicable Products

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<th>Product Name</th>
<th>Mfr. Part # (UT54ACS)</th>
<th>SMD # (5962-)</th>
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*PIC = Product Identification Code

1.0 **Overview**

The purpose of this document is to provide some background information and a brief description of the recommended operation and implementation of Redundancy and Cold Sparing using the UT65CML8X8FD Crosspoint Switch (XPS).

2.0 **Technical Background**

The generally accepted configuration for Cold Sparing is for the Primary device powered-up (ON) and active, while the Redundant device is powered-down (OFF) and inactive. For this Design Note, both the Primary and Redundant devices share a common, point-to-point signaling channel. The high-speed Inputs/Outputs (I/Os) of the Primary active devices would be toggling, which would then also present toggling signals to the inactive Redundant device high-speed I/Os.

3.0 **Cold Spare Operation**

Redundancy via Cold Sparing has been used successfully over many years for Complementary Metal Oxide Semiconductor (CMOS) and Low-Voltage Differential Signaling (LVDS) I/O logic standards. The application is in high-rel., space flight hardware, at data rates up to approximately 400 Mbps. However, Cold Sparing isn’t commonly applied to or implemented in new, high-speed, multi-Gbps Current-Mode Logic (CML) I/Os, such as in FPGA SERDES, or specifically for the XPS operating at 3.125 Gbps, for example. These new parts support the VITA 78 / SpaceVPX standard, among others. Figure 1 and Figure 2 depict the two main configurations for Cold Sparing of legacy LVDS I/O signaling standard links as part of a data link Redundancy implementation.

As shown in these figures, the Primary and Redundant Transmitter (TX) and Receiver (RX) I/Os are typically configured as separate devices, i.e.: two separate TX devices and two separate RX devices.
Figures 1 and 2 depict different configurations for the CML XPS, including proper and improper methods of achieving Redundancy for multi-Gbps CML data links.

For Figures 3 - 6, the Primary and Redundant TX (RX) channels may be on either a) two separate devices, or b) a single shared device, i.e.: one single device with two TX (RX) channels, or two separate devices with a single TX (RX) channel each. The selected configuration depends on actual redundancy implementation.

Figure 3 indicates the preferred, point-to-point data channel configuration, which uses Primary and Redundant channels and devices in a half-duplex topology. Figure 4 shows an alternate Redundancy implementation. These are the two recommended Cold Spare Mode configurations for the XPS device.
Figure 3: 3.125 Gbps CML Redundancy in Point-to-Point Signaling Channels (Recommended).

Figure 4: 3.125 Gbps CML Redundancy in Point-to-Point Signaling Channels (Optional).

The example of Figure 5 depicts a not recommended or supported redundancy configuration. There are two problems with this topology: a) The Signal Integrity (SI) of the point-to-point channel is compromised for the multi-Gbps data rate application. This is due to excessive loading and impedance mismatch and/or discontinuities from the I/O of the Redundant devices, when assuming all devices are front and back terminated to 100Ω differential load resistance. In addition, b) The Primary, active, near-end, TX output toggling when driving the Redundant, far-end, inactive, RX input when powered-off, is not supported for the Cobham XPS.
The next example as Figure 6 applies to the specific case of the Cobham XPS device, and other known similar products currently available, and has one of the same problems as given in the example of Figure 5. For the Primary channel, the active, near-end, TX output is toggling when driving the far-end, inactive, RX input when powered-off. This is not supported currently by the Cobham XPS. The limitation is due to circuit topology, including input Electrostatic Discharge (ESD) protection diodes, and the related impacts to long-term device Reliability. Active, or toggling inputs are not allowed for powered-down XPS RX inputs.
4.0  CML TX/RX Channel – XPS Notional Circuit Schematic

CML is a point-to-point signaling only logic standard. CMOS and LVDS, for example, can be point-to-point, multi-drop, or multi-point. These different topologies can be used for CMOS and LVDS I/O logic standards because they operate at much lower data rates – approximately one eighth of the CML XPS. Figure 7 shows a notional CML schematic for the Cobham XPS, and would generally apply to similar high-speed CML digital links, including other SpaceVPX/VITA 78 compatible Crosspoint Switches, SERDES, Re-drivers, Re-timers, etc. Note that all inputs are shown as AC-Coupled, which is required by many high-speed signaling protocols, such as XAUI, for example. ESD protection diodes are shown on all high-speed Inputs and Outputs (I/O).

![Notional Circuit Schematic](image)

**Figure 7: 3.125 Gbps XPS CML TX to RX Point-to-Point Channel – Notional Schematic**

5.0  Summary and Conclusion

Implementing Redundancy via Cold Sparing methods and techniques doesn’t directly translate from lower data rate CMOS and LVDS serial data links to CML multi-Gbps systems as signal integrity (SI) requirements become much more difficult to achieve. In addition, the SpaceVPX standard includes its own system-level Redundancy, and Fault Tolerance functions. Also, the primary function of the XPS IC is as an A-B Redundant switch. Therefore, in view of these considerations, Redundancy and Cold Sparing for 3.125 Gbps SpaceVPX (VITA 78) networks must be determined in the context of the overall system-level ecosystem.

For the intended A/B redundancy application, the XPS can be powered-down for Cold Sparing (VDDx=0), but for the powered-up, near-end TX device, the high-speed output must not be toggling when driving the powered-down, far-end RX device input. The XPS then only partially meets the general definition of Cold Sparing, but is similar in operation in this regard to other known, existing high-speed CML products supporting high-rel. space applications.

These are the important aspects of Cold Sparing for the XPS, in the context of SpaceVPX networks, including RapidIO multi-Gbps SERDES endpoints and Switches.
Appendix A

Preliminary Data Sheet: https://www.cobhamaes.com/pagesproduct/datasheets/UT65CML8X8FD.pdf
Current-Mode Logic (CML)
UT65CML8X8FD 3.125 Gbps Crosspoint Switch (XPS)
Preliminary Datasheet
Cobham.com/HiRel
July 16, 2018

An UT65CML8X8FD XPS Evaluation Board (EVB) is available
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