Overview

This document calculates the dynamic power dissipation capacitance for the UT54ALVC2525 Clock Driver. To focus specifically on the capacitive power dissipation of the UT54ALVC2525, this analysis removed output loading to eliminate the capacitive load power dissipation and forced fast input edge rates to reduce internal shoot through currents to a minimal value. With these constraints, essentially all of the measured AIDD current results from the internal power dissipation capacitance ($C_{pd}$) of the device. Knowing this, the designer can now accurately determine the total power dissipation of the UT54ALVC2525 Clock Driver by summing internal power dissipation capacitance ($C_{pd}$) developed in this application note with the actual capacitive load dissipation of their specific application.

The UT54ALVC2525 is a low-voltage CMOS, minimum skew, one-to-eight clock driver. The UT54ALVC2525 distributes a single clock to eight, high-drive outputs with low skew across all outputs during both the $t_{PLH}$ and $t_{PHL}$ transitions, making it ideal for signal generation and clock distribution. Since the UT54ALVC2525 is a critical component for clock and signal distribution, calculating its’ power dissipation is an important aspect of system power supply and thermal management design. Total power consumption has several components. This document calculates dynamic power-dissipation capacitance ($C_{pd}$) for the UT54ALVC2525 and shows how it contributes to the total power consumption of this device.

The two components of total power consumption for CMOS devices such as the UT54ALVC2525 are static power consumption ($P_S$) and dynamic power consumption ($P_D$). The relationship between $P_S$ and $P_D$ is expressed in Equation 1:

Equation 1

$$P_{Total} = P_S + P_D$$

Static power consumption results from leakage currents when all inputs are at constant logic values and the circuit is not changing states. Static power consumption is typically very small for CMOS devices and is estimated using data sheet values for quiescent supply current, and input leakage current. Dynamic or switching power consumption is the result of the circuit actively changing states and this is the significant contribution to the overall power consumption of the device. This document is concerned with calculating the dynamic power consumption of the UT54ALVC2525.

Dynamic power consumption for a CMOS device also has two components: transient power consumption ($P_T$) and capacitive-load power consumption ($P_L$). Equation 2 lists the components for dynamic power dissipation and then expands each to show the variables necessary to calculate their power consumption. A definition for each variable follows the equation.

Equation 2

$$P_D = P_T + P_L = (C_{pd} * V_{DD}^2 * f) + (C_L * V_{OUT,PP}^2 * f_O * N_{SW})$$

Where:

$P_D$ = dynamic power consumption

$P_T$ = transient power consumption
The transient power consumption \( P_T \) results from currents flowing within the device when internal transistors switch states during operation. This includes both the actual switching currents required to charge the internal nodes and the shoot-through or crowbar currents that flow through a CMOS device when both p-channel and n-channel transistors briefly conduct during switching. The frequency at which the device switches, as well as the rise and fall times of the switching signals, has a direct effect on the transient power dissipation. For fast rise and fall times, the shoot-through currents are small compared to the switching currents required to charge the internal nodes. For this analysis, we use a 1ns rise/fall time for the input reference clock to minimize these shoot-through currents. Thus, the switching of the internal capacitance of the device, known as the dynamic power dissipation capacitance \( C_{pd} \), determines the UT54ALVC2525 transient power dissipation.

The capacitive load portion \( P_L \) of the dynamic power consumption \( P_D \) results from actively charging and discharging output capacitive loads. This depends on the external loading and the switching frequency of the output drivers. To calculate capacitive load power dissipation, the user must determine the number of outputs switching, their frequency of operation and the actual peak-peak switching voltage at each load. Since the purpose of this analysis is to determine the internal, dynamic power dissipation \( C_{pd} \) for the UT54ALVC2525, we use a characterization board with output pins lifted so the load capacitance on each output \( C_L \) is negligible. This removes the capacitive load portion of the dynamic power dissipation, leaving only the transient power dissipation defined by the dynamic power dissipation capacitance in Equation 2. The short pins also ensure no reflections or “ringing” on the output signals that would increase the measured currents.

The remaining discussion uses this reduced equation for power dissipation to calculate \( C_{pd} \) for the UT54ALVC2525. Equation 3 shows the dynamic power dissipation solved to calculate \( C_{pd} \).

**Equation 3**

\[
P_D = P_T + P_L = P_T = (C_{pd} \cdot V_{DD}^2 \cdot f_I): \text{ for fast input rise/fall and } C_L \approx 0pF
\]

\[
P_D = (V_{DD})^2(I_{DD}) = (C_{pd} \cdot V_{DD}^2 \cdot f_I)
\]

\[
C_{pd} = (V_{DD} \cdot I_{DD}) / (V_{DD}^2 \cdot f_I)
\]

\[
C_{pd} = I_{DD} / (V_{DD} \cdot f_I)
\]

2 Technical Data

To determine \( C_{pd} \) in the laboratory, measure the \( I_{DD} \) supplied to the device across its frequency range of operation, then calculate an average \( I_{DD} / f_I \) slope. The data in Table 2 lists this active current (AIDD), measured versus frequency for the UT54ALVC2525. AIDD values are from maximum measurements taken during characterization of a single UT54ALVC2525 device configured under the following conditions. Each set of data points calculates an AIDD/frequency slope. The data and corresponding AIDD/frequency slopes appear in Figure 1. Table 1 summarizes an average value for \( \text{Cpd} \) at each of the three temperatures. Please note the listed conditions for the lab characterization.
Device: UT54ALVC2525

Temperature: \( T_C = 25^\circ C, +125^\circ C, -55^\circ C, \)

Voltage: \( V_{DD} = 3.3 \) V

Frequency: \( f = 1 \) MHz, 25 MHz, 50 MHz, 75 MHz, 100 MHz, 125 MHz, 150 MHz, 175 MHz, 200 MHz

Table 1 UT54ALVC2525 \( C_{pd} \) Characterization Data

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>AIDD (mA) -55°C</th>
<th>Slope (mA/MHz)</th>
<th>AIDD (mA) 25°C</th>
<th>Slope (mA/MHz)</th>
<th>AIDD (mA) 125°C</th>
<th>Slope (mA/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UT54ALVC2525 Clock Buffer Vdd= 3.3V Input rise/fall time &lt; 1ns ( C_{L(\text{eff})} = 0 ) pF</td>
<td>0</td>
<td>0.054</td>
<td>0.047</td>
<td>0.044</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.592</td>
<td>0.624</td>
<td>0.710</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>12.19</td>
<td>0.483</td>
<td>12.37</td>
<td>0.489</td>
<td>13.11</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>23.68</td>
<td>0.460</td>
<td>24.24</td>
<td>0.475</td>
<td>25.12</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>32.46</td>
<td>0.351</td>
<td>33.57</td>
<td>0.373</td>
<td>35.28</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>46.13</td>
<td>0.547</td>
<td>47.17</td>
<td>0.544</td>
<td>48.73</td>
</tr>
<tr>
<td></td>
<td>125</td>
<td>56.66</td>
<td>0.421</td>
<td>57.41</td>
<td>0.410</td>
<td>59.26</td>
</tr>
<tr>
<td></td>
<td>150</td>
<td>66.05</td>
<td>0.376</td>
<td>67.33</td>
<td>0.397</td>
<td>69.33</td>
</tr>
<tr>
<td></td>
<td>175</td>
<td>75.25</td>
<td>0.368</td>
<td>76.55</td>
<td>0.369</td>
<td>78.61</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>84.25</td>
<td>0.360</td>
<td>85.57</td>
<td>0.361</td>
<td>87.40</td>
</tr>
<tr>
<td>Slope Average (mA/MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.421</td>
<td>0.427</td>
</tr>
</tbody>
</table>

\( C_{pd} \) (pF)

| | 127.487 | 129.448 | 132.131 |

Figure 1.1 UT54ALVC2525 Characterization Plots: AIDD vs. Frequency