UTMC APPLICATION NOTE

UT69RH051 Address/Data Demultiplexer

UTMC recommends the following circuit to demultiplex address from data during UT69RH051 external memory and instruction cycles. The circuit uses UT69RH051 output ALE to control a flip-flop. D flip-flop outputs (Q_N) equal inputs (D_N) when ALE transitions from high to low. Port 0 outputs from the UT69RH051 supply the least significant 8 bits address information and drive flip-flop inputs D_N. Port 2 outputs supply the upper 8 bits of address information. Flip-flop outputs D_N, in combination with Port 2, drive memory address inputs A(15:0). The combination of Port 0 and 2 allows the UT69RH051 to access a 64K memory space.

Address information from Port 0 and 2 is valid \( t_{AVLL} \) (\( t_{CLCL} \)-40ns minimum) before the falling edge of ALE. During 20MHz operation, address information becomes valid at least 10ns before the falling edge of ALE. The maximum propagation delay from D_N to Q_N for the UT54ACS374 is 18ns. The maximum propagation delay from D_N to Q_N for the UT54ACS14 is 14ns. Therefore, 32ns after the falling edge of ALE, the D-flip-flop presents valid address information to the memory. The memory array must return read information within \( t_{LLIV} \) for a valid program instruction and \( t_{LLDV} \) for a data memory read. Subtracting 32ns from both \( t_{LLIV} \) and \( t_{LLDV} \) leaves 68ns for program instruction reads and 218ns minimum for data memory reads. The 68ns and 218ns determines the access time requirements for a program instruction fetch and a read of program memory. The UT54ACTS374 requires at least 5ns of data setup prior to the falling edge of the input clock. The worst case relationship between Port 0 valid and ALE low meets this requirement. Figure 1 displays the recommended circuit.

![Figure 1. UT69RH051 Address and Data Demultiplex Circuit](image)

Use PSEN and/or RD to control the memory output enable function. The memory array output enable assertion to valid data must meet requirements \( t_{PLIV} \) and \( t_{RLDV} \). At 20MHz, the memory array must return valid data within 45ns of the PSEN assertion or within 85ns of the RD assertion. A simple logical “AND” of PSEN and RD generates a memory array output enable. The memory array successfully write with a minimum write strobe width of \( t_{WLWH} \) of 200ns at 20MHz. Use UT69RH051 output WR to control the memory array write input.
To increase noise immunity choose a CMOS input Dflip-flop (i.e., UT54ACS374). $V_{\text{OH}}$ minimum (4.2 volts) for both Port 0 and ALE meets the UT54ACS374’s $V_{\text{IH}}$ minimum of $0.7V_{\text{DD}}$ (3.85 volts @5.5 $V_{\text{DD}}$). $V_{\text{OL}}$ maximum (.3 volts) for both Port 0 and ALE meets the UT54ACS373’s $V_{\text{IH}}$ maximum of $0.3V_{\text{DD}}$ (1.65 volts @5.5 $V_{\text{DD}}$). The CMOS D-flip-flop drives within 250mV of $V_{\text{SS}}$ or $V_{\text{DD}}$ (i.e., $V_{\text{SS}}+.25$ or $V_{\text{DD}}-.25$) while sinking ($I_{\text{OL}}$) or sourcing ($I_{\text{OH}}$) 100mA.